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Complementary Bodydriving - A Low-voltage Analog Circuit Technique Realized In 0.35um SOI Process

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To the Graduate Council:

I am submitting herewith a thesis written by Yong LeeKee entitled "Complementary Bodydriving - A Low-voltage Analog Circuit Technique Realized In 0.35um SOI Process." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this thesis and recommend its acceptance:

Donald W. Bouldin, Syed K. Islam

Accepted for the Council:

Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Syed K. Islam

Accepted for the council:

Anne Mayhew

Vice Provost and Dean of Graduate
Studies

(Original signatures are on file with official student records.)

Complementary Body-driving - A Low-voltage Analog Circuit Technique Realized In 0.35um SOI Process

A Thesis
Presented for the
Master of Science
Degree

The University of Tennessee, Knoxville

LeeKee Yong
August 2002

Dedicated to my family and friends who
have motivated and supported me
throughout my college career.

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Abstract

This thesis presents a study of several analog circuit primitives that utilize the body terminal as a signal port to achieve low-voltage operation and high performance. Several issues relating to low-voltage applications as well as the trends of technology scaling in the near future are presented. Principles of the body-driven transistor for both PMOS and NMOS in PDSOI technology are described, and critical design considerations are discussed. The design of low-voltage analog primitives (cascode current mirror and differential pair) are described and analyzed in detail. A discussion of the design and analysis of a 4-quadrant analog multiplier is also presented. Prototyping and testing procedures are discussed and the results of the prototyped circuits are evaluated. Finally, a summary of the work is presented along with insights gained toward future research.

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Chapter 1

Introduction and Overview

In today's ever-changing technology environment coupled with the explosive growth in portable electronics market, the general emphasis in VLSI (Very Large Scale Integration) is gradually shifting away from high speed to low power circuitry. Low power CMOS design has become more of a necessity rather than a niche design skill previously limited to battery operated applications [1]. The increase in package density and faster clock frequencies have forced the issues of heat removal and power dissipation to the forefront of integrated circuit (IC) design. Analog and digital circuit designers today are struggling to design high performance yet low power circuits for virtually every mainstream design application.

In order to minimize power dissipation, one intuitive way is to reduce the supply voltage since low- V_{DD} is advantageous for achieving low dynamic power dissipation in digital circuits [2]. Lower supply voltage is also needed to ensure sufficient transistor reliability in deep sub-micron processes. Thus, analog circuitry must be designed around this design trade-off, causing most of the traditional design techniques such as cascode amplifier stages to become impractical. Therefore, alternatives to these challenges must be examined. The low-voltage primitives presented in this thesis predominantly focus on low-voltage circuit design in PDSOI (Partially-Depleted Silicon-On-Insulator) technology using the body terminal as a signal port. One should find wide application of this technique in next generation CMOS analog circuit designs.

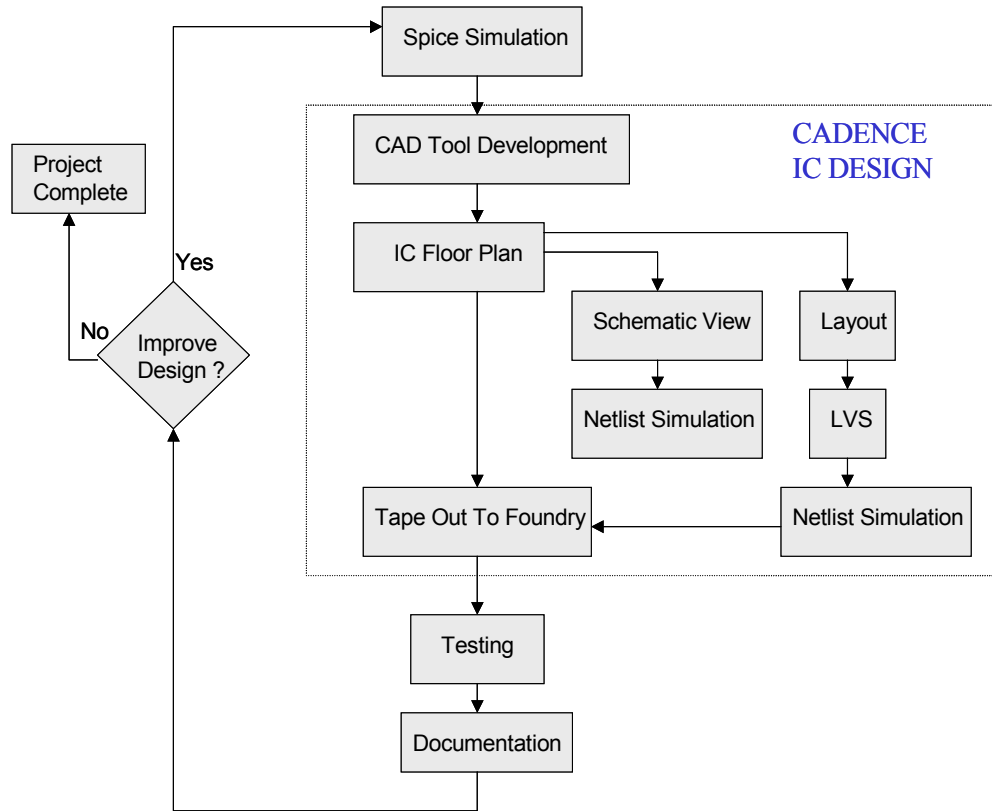


Figure 1.1: Risk Reduction IC Design Cycle

The design cycle for the prototype circuits resulting from this work is illustrated in Figure 1.1. This design cycle is structured for risk reduction with respect to expensive fab iteration. Multiple simulation stages have been included in every cycle to fine tune the design and reduce circuit uncertainties, such as parasitics (e.g., parasitic capacitance) and human errors. Circuit testing is done after the IC has returned from the fabrication foundry and the measured results are compared to simulations. If necessary, the second phase of the design cycle begins and the improved design will be fabricated again. This thesis documents the measurement results and conclusions from the first prototype cycle fabricated through a commercially available PDSOI foundry.

This thesis contains 4 chapters. Chapter 2 discusses technology trends and presents the theory and measured results of the body-driven transistor in PDSOI for both n-type and p-type MOSFETs as alternatives for low-voltage applications. Low-voltage analog primitives such as the cascode current mirror, 4-quadrant analog multiplier, and constant transconductance fully complementary differential input gain stage using body-driving are presented in chapter 3. A summary of simulation results versus measured results is also included in chapter 3. Chapter 4 summarizes the work herein and suggests future direction. The subsequent appendices provide a full circuit library listing including simulation input files, IC microphotographs, and test setup photographs.

Chapter 2

Body-Driven MOSFET in PDSOI

This chapter discusses the theory and analysis of the body-driven transistor, both NMOS and PMOS, on a 0.35-um PDSOI process. The bulk or body-driving technique is also introduced in contrast to the conventional gate-driven technique to demonstrate its low-voltage capability.

2.1 Technology Scaling

Technology scaling has enabled great advancements in the performance of both analog and digital integrated circuits. It is well known that shrinking feature sizes have increased intrinsic device speed, and lower power supply voltage can reduce the dynamic power dissipation of digital circuits. Dynamic power dissipation is the energy used when the circuit transitions from high-to-low and vice versa, and can be described by [8]

$$P_{dynamic} \propto (f_{clk} \cdot V_{DD}^2) \quad 2.1$$

where f_{clk} is the clock frequency and V_{DD} is the supply voltage. However, reduction in power supply voltage has complicated analog circuit design because the threshold voltages, V_{TP} and V_{TN} , do not scale accordingly and thus cause a severe penalty in circuit dynamic range. Current generation analog circuit designs, which operate at 2.5V and 3.3V, routinely use wide dynamic range current mirrors and rail-to-rail transconductors [6]. However, these techniques are not applicable when power supply voltage is below $|V_{TP}| + |V_{TN}|$ [1].

2.2 Low-Voltage Design with Body-Driving

The fundamental problem for the modern, low-voltage analog circuit designer is that threshold voltage does not scale with power supply voltage. In fact, it is predicted that by 2004 power supply voltage will reach 1.0V while threshold voltage will be as high as 0.5V [7]. Obviously circuit design techniques that are not limited to operation above $|V_{TP}| + |V_{TN}|$ must be investigated [1]. One very promising low-voltage technique is to utilize the transistor's body as a signal input. Body-driven circuits have been successfully implemented in bulk CMOS where a 1.0V op-amp was reported in a standard 2- μm digital bulk CMOS technology [4, 5]. However, a fundamental limitation of body-driven circuits in bulk CMOS is that complementary body-driving (for NMOS and PMOS at the same time) is not possible since the native substrate is a shared body terminal for all the NMOS transistors (assuming a p-type substrate). Therefore partially-depleted (or thick-film) SOI, which provides an isolated body contact for every device, enables complementary body-driven circuits and is thus an ideal vehicle for implementing body-driven circuits. Low-voltage in SOI also offers many advantages over its bulk CMOS counterpart. It offers reduced influence of short-channel effects, lower substrate leakage current, lower parasitic capacitance, greater temperature insensitivity, and potentially lower threshold voltage [1].

2.3 Voltage Budget for Conventional Gate-Driven Transistor

The minimum voltage for a MOSFET to turn-on operating in strong inversion and processing an analog signal applied to its gate is described by [4]

$$V_{DD} + |V_{SS}| \geq V_{GS} = V_{DS, SAT} + |V_T| + V_{signal} \quad 2.2$$

where V_{DD} and V_{SS} are the most positive and negative supply voltage, respectively [1]. $V_{DS,SAT}$ is the minimum drain-to-source voltage required for saturation operation and from MOSFET square-law first-order theory is given by [6]

$$V_{DS,SAT} = \sqrt{\frac{2I_D}{\mu C_{OX}(W/L)}} = V_{GS} - |V_T| \quad 2.3$$

where I_D is drain current, μ is carrier mobility, C_{OX} is gate-oxide capacitance for the process, V_{GS} is gate-to-source voltage, and V_T is threshold voltage for the MOS transistor [3]. Expression 2.2 reveals how signal swing, and therefore dynamic range, is constrained by the turn-on or threshold voltage of the MOSFET. In practice, the minimum $V_{DS,SAT}$ for the n-type MOSFET is about 100mV to saturate and about 250mV for strong inversion saturation. Thus, the minimum supply voltage for the gate-driven NMOS transistor alone is already 0.9V for a V_T of 0.65V. This is a severe performance limitation for low-voltage analog circuits.

2.4 Body-Driven N-type MOSFET in PDSOI

The body-driven MOSFET described below (Figure 2.1) provides an attractive solution to the turn-on voltage limitation without specialized processing. In PDSOI CMOS, an individual transistor can be body-driven because of the oxide isolation provided by buried oxide (BOX) and field oxide (FOX). Unlike bulk CMOS technology, the parasitic vertical bipolar junction transistor is completely annihilated because of the BOX layer. Turn-on condition of the parasitic lateral bipolar junction transistor, however, must be avoided when the MOSFET is body-driven. The operation of the body-driven MOSFET is much

like a JFET. To enable body-driving, one must first bias the gate to form a conduction channel inversion layer by connecting the gate terminal to a fixed voltage that is sufficient to form an inversion layer (e.g., $V_{GS} > V_T$ for the NMOS). By applying a potential difference between the drain and source, this inversion layer will act very much like a conduction channel of JFET. Since the body voltage affects the thickness of the depletion region associated with the inversion layer (conduction channel), the drain current can be modulated by varying the body voltage through the body effect of the MOSFET. From MOSFET square-law first-order theory, the NMOS drain current versus body voltage for this condition is described by

$$I_D = \frac{\beta}{2} \cdot [V_{od0} - (\gamma \cdot \sqrt{2 \cdot |\phi_F| - V_{BS}}) + \gamma \cdot \sqrt{2 \cdot |\phi_F|}]^2 \quad 2.4$$

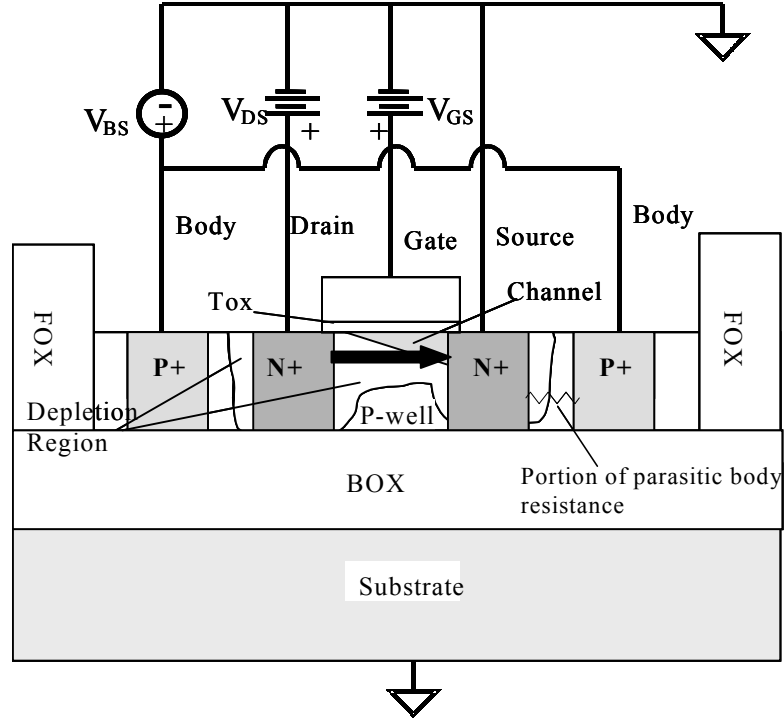


Figure 2.1: Cross Sectional of N-channel MOSFET of PDSOI CMOS Process

where gate overdrive voltage $V_{od0} = V_{GS} - |V_{TOn}|$, ϕ_F is the body surface potential, and V_{BS} is body-to-source voltage which here can be negative or positive. V_{TOn} is the NMOS threshold voltage when $V_{BS}=0V$. γ is the body effect coefficient or the body factor which is given by [8]

$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_A}}{C'_{ox}} \quad 2.5$$

where q is the electron charge, ϵ_{si} is the dielectric constant of silicon, N_A is doping concentration, and C'_{ox} is the gate oxide capacitance per unit area. β is the transconductance parameter described by [8]

$$\beta = \frac{K'W}{L} = (\mu C'_{ox}) \cdot \frac{W}{L} \quad 2.6$$

where W is the gate width and L is the length of the transistor. From equation 2.4 the channel current can be modulated using the body-to-source voltage [3]. A plot of multiple measured I_D versus V_{DS} characteristics with different V_{BS} levels for 40um/4um (4 gate finger device with $W/L=10/4$ per gate finger), 120um/2um (12 gate finger device with $W/L=10/2$ per gate finger), and 120um/4um (12 gate finger device with $W/L=10/2$ per gate finger) n-channel MOSFETs fabricated on a commercially available 0.35um PDSOI process is shown in Figure 2.2. The data indicates that using a weakly forward-biased body-to-source junction potential and gate-to-source potential held at 0.6V, only 0.2V V_{DS} is required for this body-driven transistor to achieve saturation. Figure 2.3 demonstrates drain current modulation using forward-biased body-to-source junction potential with gate-to-source voltage steps from 0.2V to 1V (from weak inversion to strong inversion), and drain-to-source voltage held constant at 1V. Note that when V_{BS} is 0.5V, the body

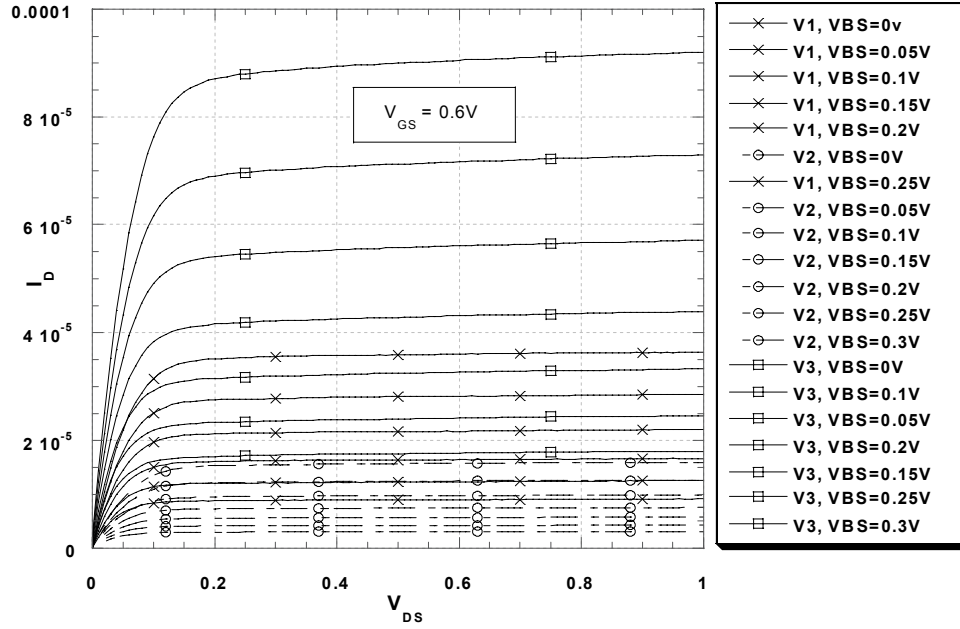


Figure 2.2: Measured I-V Curves of 40/4(v2), 120/2(v3), and 120/4(v1) BDNMOS

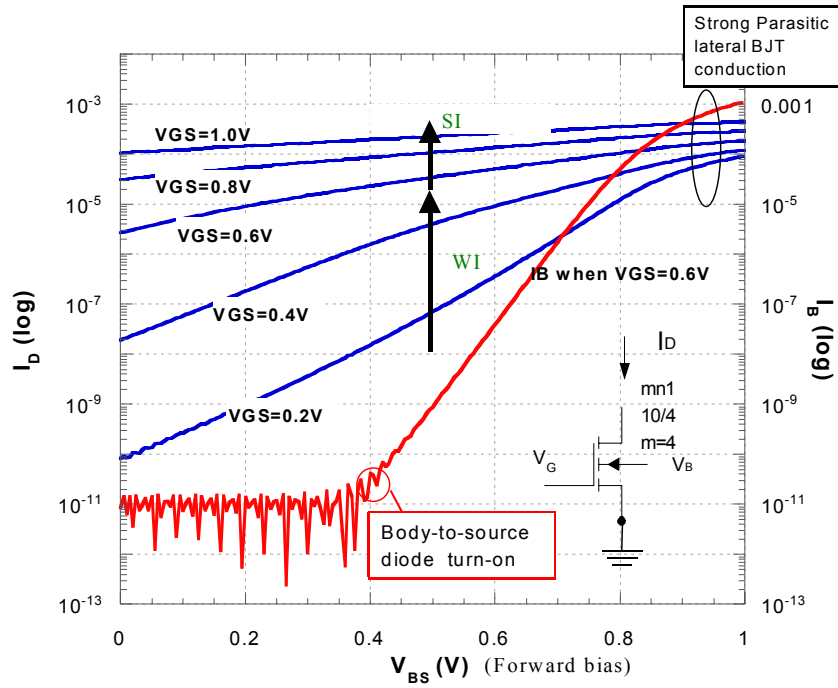


Figure 2.3: I_B and I_D versus V_{BS} for 40/4 NMOS

or bulk current is only about 1nA, which is very small for a large body area device such as this. Note that for V_{BS} less than 0.4V, the body current is extremely small. When the body-to-source diode is heavily forward-biased the body current will exponentially increase and eventually parasitic lateral BJT conduction will dominate. Thus, during normal body-driving, care is taken to avoid excessive forward-bias on the body-source junction to minimize body current and prevent the parasitic lateral BJT from turning on (often referred to as “snap back” in the SOI community [9]).

Careful examination of Figure 2.1 reveals that, the parasitic body resistance could be a significant design issue due to the high sheet resistance of MOSFET body regions ($>1k\Omega/\text{square}$). This body resistance can be minimized through careful layout with multiple gate fingers and generous use of body contacts surrounding the device. Figure 2.4 shows two sample layout structures of PDSOI NMOS transistors using this special layout technique for all of the body-driven devices and circuits described in this work.

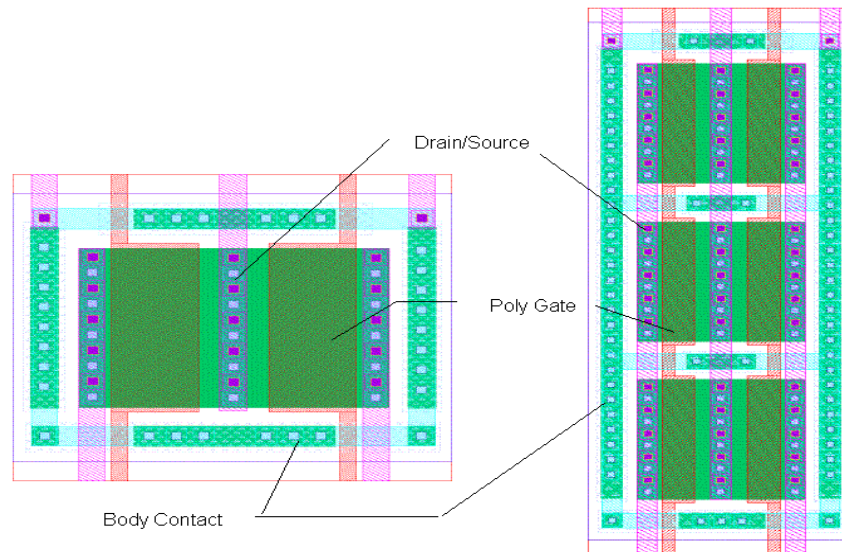


Figure 2.4: Layout Sample for PDSOI NMOS Transistor

2.5 Body-Driven P-type MOSFET in PDSOI

Body-driving a PMOS transistor together with a NMOS transistor in the same IC is made possible only in SOI technology. As mentioned previously, the FOX and BOX in SOI isolate each transistor's well (body) area from one another and from the substrate, respectively.

Figure 2.5 shows a cross sectional view of a PDSOI PMOS transistor. Just as with its NMOS counterpart, drain current modulation is achieved through body effect. Similar to body-driving the NMOS, equation 2.4 can be used to describe the drain current versus body-to-source voltage relationship (simply swap order of subscripts for correct polarity of input variables).

Figure 2.6 shows the measured I_D versus V_{SD} characteristic with different V_{SB} for 40um/4um, 120um/2um, and 120um/4um p-channel MOSFETs fabricated in a commercial 0.35um PDSOI process. With forward-bias applied to the source-to-body diode, and with V_{SG} held constant at 1.0V, only 0.25V V_{SD} is required for a p-type body-driven transistor to achieve saturation. Figure 2.7 shows the measured drain current modulation of a 40um/4um PMOS transistor achieved by applying V_B from 0 to 1V ($V_S=1V$), with V_{SG} steps from 0.2V to 1V, and source-to-drain voltage held constant at 1V. Note that when V_{SB} is 0.5V, the body current is only 1nA, again providing a high input impedance device well suited for low-voltage applications. The body resistance of the body-driven PDSOI PMOS can also be reduced by generously surrounding the device with body contacts. Figure 2.8 provides an example PMOS layout structure using this layout technique.

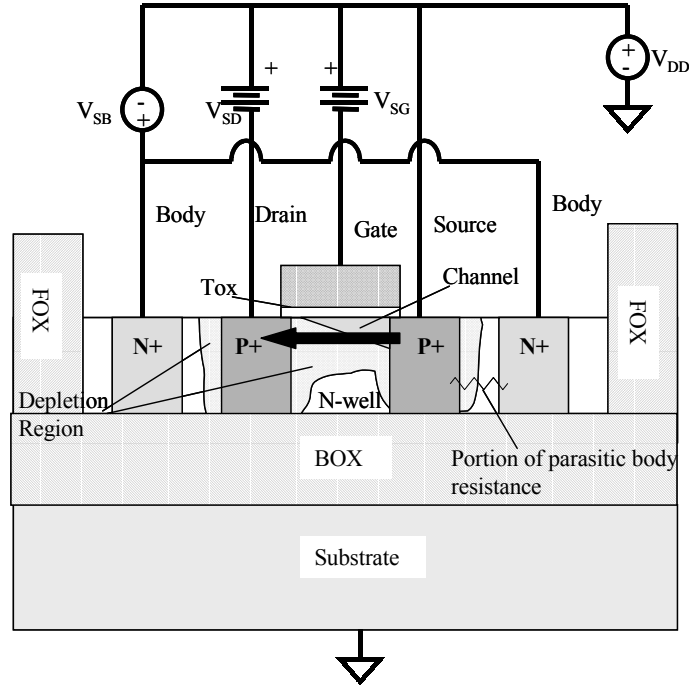


Figure 2.5: Cross Sectional of P-channel MOSFET of PDSOI CMOS Process.

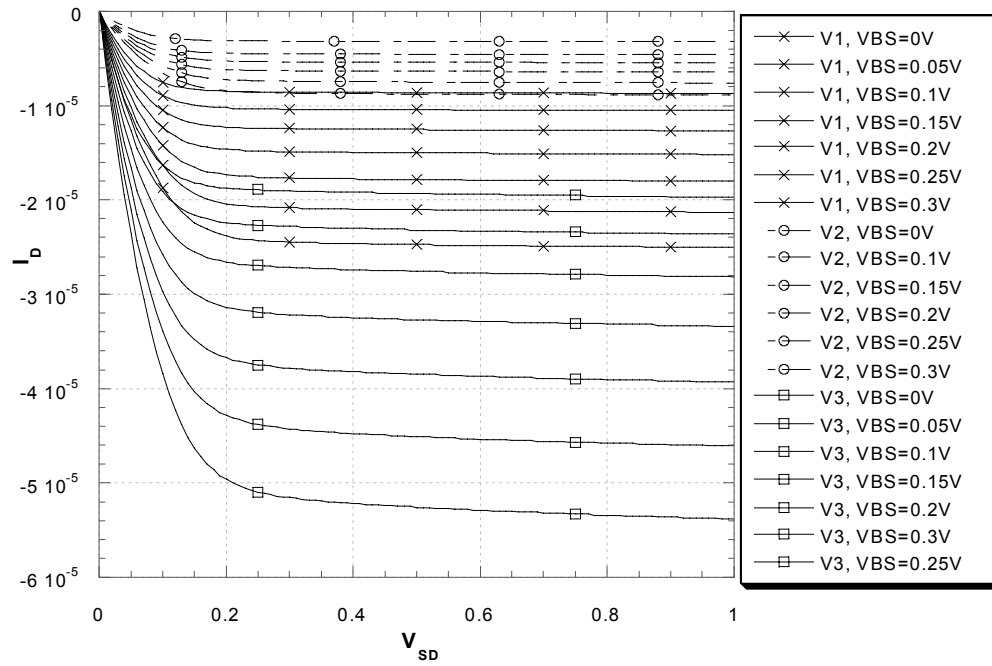


Figure 2.6: Measured I-V Curves of 40/4(v2), 120/2(v3), and 120/4(v1) BDPMOS

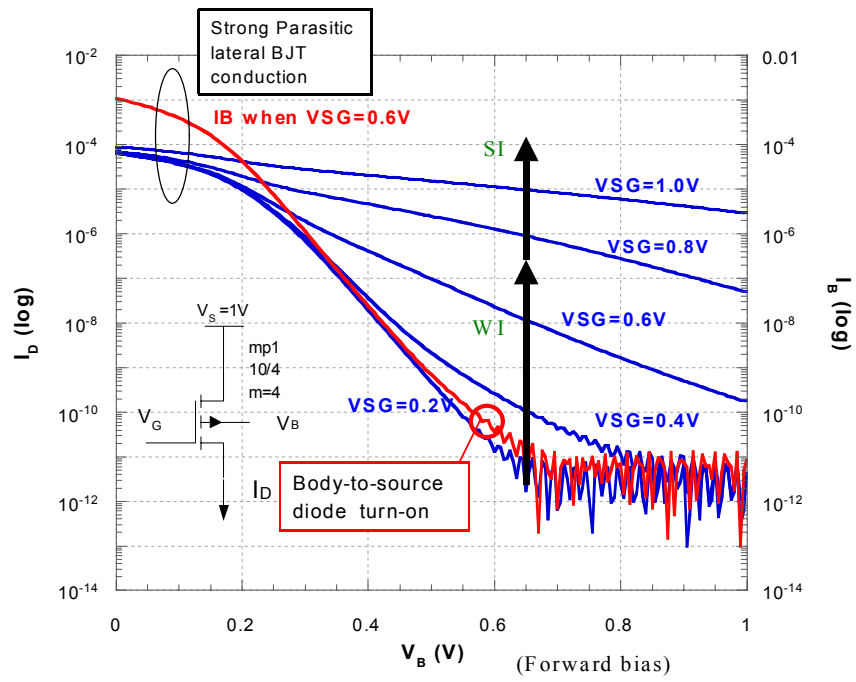


Figure 2.7: I_B and I_D versus V_B for 40/4 PMOS

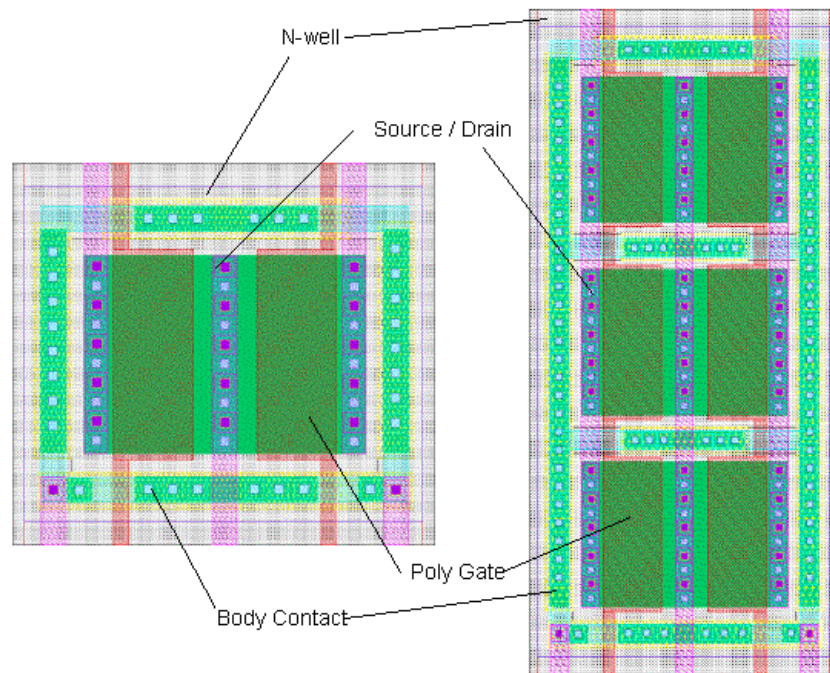


Figure 2.8: Sample Layout for PMOS Transistors in PDSOI

2.6 f_T Comparison for Gate-Driven versus Body-Driven

The unity current gain transition frequency, f_T , is defined as the frequency at which unity-gain is achieved in the common-source configuration [6]. It is a figure of merit that is taken as a rough indication of the MOSFET's high-frequency performance. From [10], f_T is estimated by the small-signal ratio of drain current to gate current

$$f_T = \frac{\omega_T}{2\pi} = \left| \frac{i_d}{i_{in}} \right| \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad 2.7$$

where $C_{gs} + C_{gd}$ is the input capacitance when the gate is used as the input terminal in this configuration. When body-driving, this input capacitance will be $C_{bs} + C_{bd}$, where C_{bs} is the depletion capacitance of the slightly forward-biased (or reversed-biased) body-to-source diode and C_{bd} is the depletion capacitance of the reversed-biased body-to-drain diode. Earlier work demonstrated that the input capacitance when body-driving is more than 3 times larger than the input capacitance when gate-driving for a given device in bulk CMOS technology [3]. However, it is well known that the body-to-source capacitance and body-to-drain capacitance in PDSOI is much less than that of a bulk CMOS transistor because of the buried oxide [1]. Consequently, this work investigates and compares the f_T associated with body-driving versus gate-driving in PDSOI.

A simple way to experimentally determine f_T is to measure the unity crossover frequency of a common-source transistor. The fundamental problem with this technique is that high frequency measurement is almost always limited by test equipment and test board parasitics since f_T is easily in the hundreds of MHz range or higher. One possible measurement setup is shown in Figure 2.9 that allows the measurement of g_m and C_{in} .

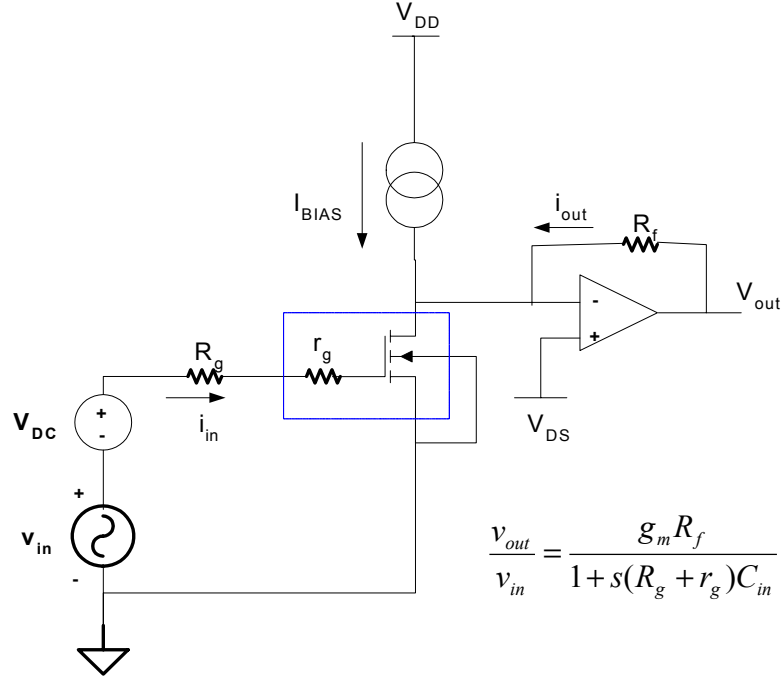


Figure 2.9: Schematic of f_T Measurement

The transfer function of this circuit is

$$\frac{i_{out}}{i_{in}} = \frac{g_m}{1 + s(R_g + r_g)C_{in}} \quad 2.8$$

where r_g is the parasitic resistance associated with the polysilicon gate of the MOSFET. The external (off-chip) resistor R_g is used to limit the current available to charge C_{in} . Since R_g can be made arbitrarily large, it is possible to make the $R_g C_{in}$ time constant arbitrary large, therefore providing a relatively low bandwidth measurement system. A similar measurement setup can be used to measure f_T when body-driving. V_{DS} can be set to ensure the transistor is always biased in saturation and hence, C_{in} will be dominated by C_{gs} [14]. For practical purposes, r_g (gate-driving) or r_b (body-driving) can be assumed negligibly small compared to R_g (gate-driving) or R_b (body-driving). Figure 2.10 and Figure 2.11 contain the f_T measurement results of an n-type PDSOI transistor

with aspect ratio of 800/5 when gate-driven and body-driven, respectively. R_f and R_g is $2k\Omega$ and $317k\Omega$, respectively, and the input signal is set to $50mV_{p-p}$ when gate-driven. When body-driven, R_f is changed to $6.15k\Omega$ to provide extra gain for the system to compensate for the smaller g_{mb} value ($g_{mb} < g_m$). The measured 3-dB roll-off frequency for $V_{GS}=0.7V$ and $V_{BS}=0V$ is summarized in Table 2.1. Using measured f_{-3dB} values, the calculated $C_{in,body}$ is found to be only 1.26 times greater than $C_{in,gate}$, which is much smaller than the $C_{in,body}$ to $C_{in,gate}$ ratio of about 3.8 for bulk CMOS technology reported in [3, 4]. Thus, there is nearly a 3X reduction in input capacitance penalty when body-driving in PDSOI compared to bulk CMOS. The average measured C_{gs} is about 14.6pF and the average measured C_{bs} is approximately 20.8pF, depending on the gate bias condition for the PDSOI 800/5 NMOS device tested. Regarding transconductance, first-order theory stipulates that g_{mb} increases linearly with g_m , and g_m is a function of V_{GS} [6]. Based on Figure 2.11 and [3], the f_T , body-driven for PDSOI can be described by

$$f_{T, body-driven} = \frac{\eta}{1.26} f_{T, gate-driven} \quad 2.9$$

where η is the ratio of g_{mb} to g_m . This demonstrates that the f_T when body-driving is about 3X higher in PDSOI compared to the f_T estimation derived in [3] based on bulk CMOS (assuming comparable η value).

Table 2.1: Measured f_T for Gate-Driven and Body-Driven PDSOI 800/5 NMOS.

	$g_m = V_{out}/R_f V_{in}$	$C_{in,gate} = (2\pi R_g f_{-3dB})^{-1}$	$f_{T,gate} = g_m / (2\pi C_{in,gate})$
gate-driven	2.05mS	14.8pF	22.1MHz
	$g_{mb} = V_{out}/R_f V_{in}$	$C_{in,body} = (2\pi R_b f_{-3dB})^{-1}$	$f_{T,body} = g_{mb} / (2\pi C_{in,body})$
body-driven	900 μ S	18.6pF	7.7MHz

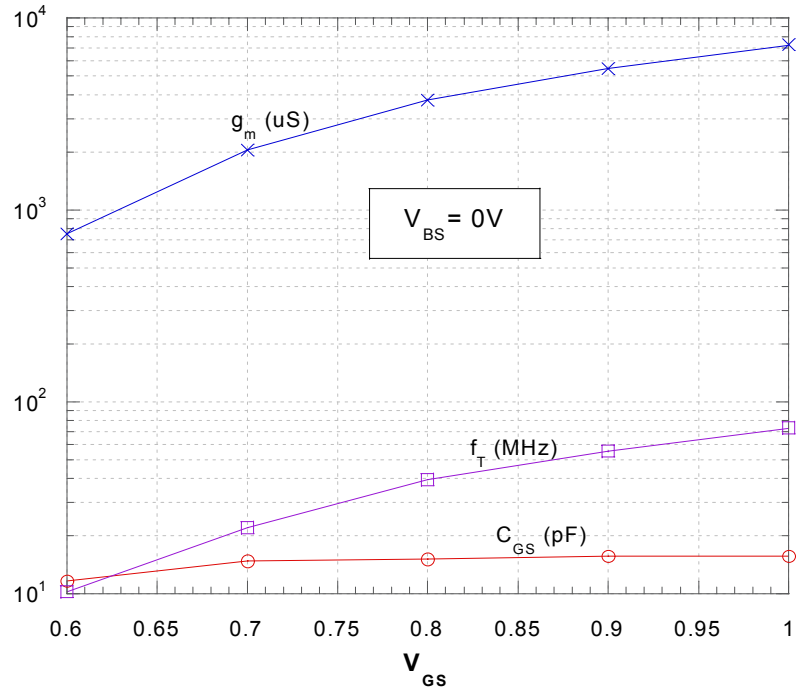


Figure 2.10: Measured f_T Plot for Gate-Driven 800/5 NMOS in PDSOI.

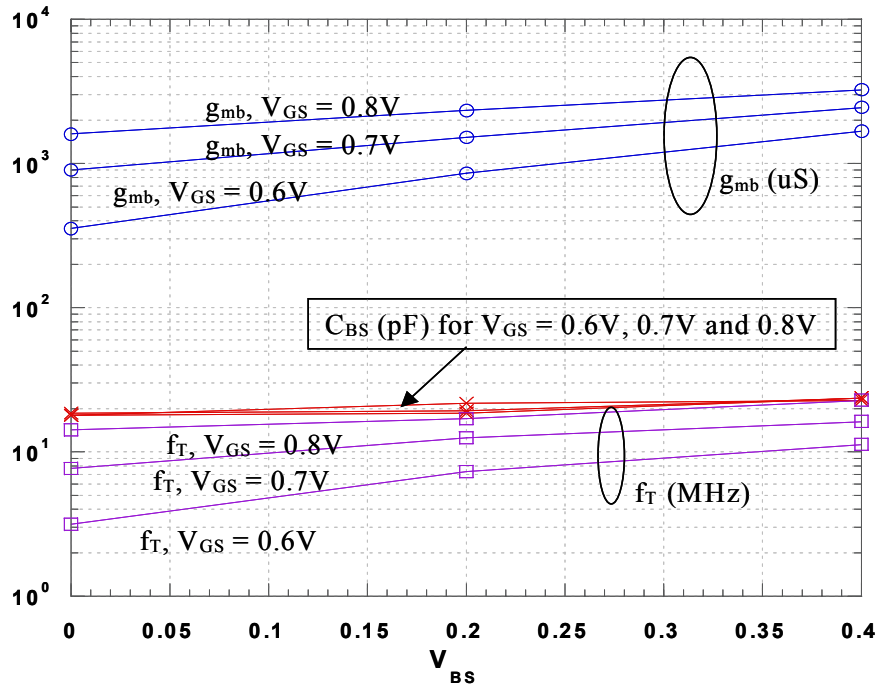


Figure 2.11: Measured f_T Plot for Body-Driven 800/5 NMOS in PDSOI.

Chapter 3

Body-Driven Analog Primitives in 0.35 PDSOI

This chapter introduces some key building block circuits for the design and implementation of ultra low supply voltage analog systems using the body-driving technique. Basic circuits such as the body-driven cascode current mirror, differential pair, and analog multiplier for both p- and n-type circuits are demonstrated through simulation and measurement results.

3.1 Body-Driven Cascode Current Mirror (BDCCM) in PDSOI

3.1.1 Theory

The current mirror is a commonly used circuit block in analog design. It is well known that the input voltage, V_{IN} , required for a gate-driven simple current mirror with gate-to-drain connected input device will be at least 250mV above V_T for strong inversion saturation operation, which could easily be 0.9V to 1.0V [8]. To improve the current matching performance over process corners and also output impedance, a cascode current mirror is preferable. One drawback of the gate-driven standard cascode current mirror is the output voltage requirement is at least 500mV above V_T and the input voltage requirement is at least 500mV above $2V_T$ for strong inversion saturation operation, which can easily be 1.2V and 1.9V, respectively [8]. Analog circuit engineers are forced to design circuits around this limitation use more complicated topologies such as the wide-swing cascode

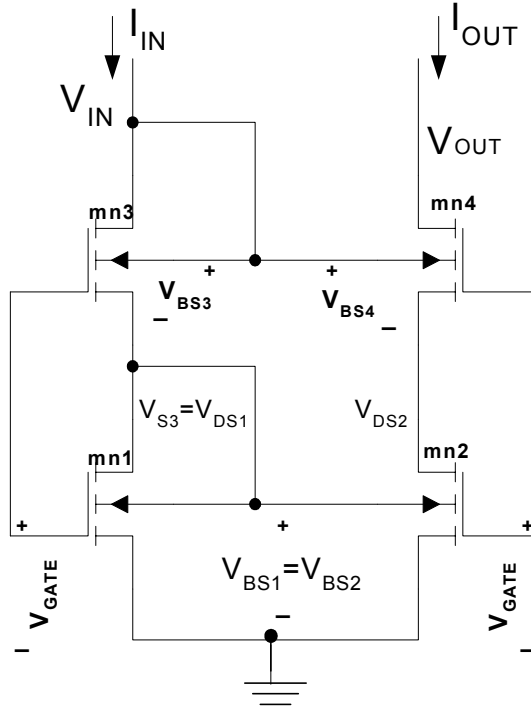


Figure 3.1: N-type BDCCM Circuit Block

[6]. Due to this increase in design complexity, design time is also increasing. A simple n-type cascode body-driven current mirror, shown in Figure 3.1, can be used as an alternative to remove the threshold voltage limitation at both V_{IN} and V_{OUT} . Note that a p-type version can be readily implemented and will be discussed in a later section. As described in section 2.2, all of the MOSFET gate terminals are fixed at potential V_{GATE} to provide a conduction channel between each drain and source. The body terminals are utilized for biasing and drain current is established by weakly forward biasing the body-to-source junctions of the NMOS transistors. By inspection, we can conclude that $V_{DS2} = V_{DS1} + V_{BS3} - V_{BS4}$, $V_{GS1} = V_{GS2}$, $V_{BS1} = V_{BS2}$, as well as $V_{BS1} = V_{DS1}$ and $V_{BS3} = V_{DS3}$. When $I_{IN} > I_{DSS, mn1}$ and $V_{BS1} > 0V$, the body-to-source junctions of mn1 and mn2 are

1. I_{DSS} is the saturation drain current when $V_{BS}=0V$ for a given V_{GS} bias.

(preferably weakly) forward-biased. If mn3 is sized to match mn1, then $I_{DSS,mn3} = I_{DSS,mn1}$ and V_{DS2} will be greater than 0V since V_{DS1} is positive. This establishes $V_{DS2} + V_{BS4} > 0V$ and mn2 will begin conducting since $V_{DS2} > 0V$ when $I_{IN} > I_{DSS,mn1}$. The aforementioned conditions, particularly $V_{DS1} + V_{BS3} = V_{DS2} + V_{BS4}$ and device matching, in addition to DC negative feedback, force $I_{IN} = I_{OUT}$ (once mn2 is conducting after the $I_{IN} > I_{DSS,mn1}$ condition is met). The input voltage V_{IN} and output voltage V_{OUT} can be described by

$$V_{IN} = V_{BS1} + V_{BS3} \quad 3.1$$

$$V_{OUT(MIN)} = V_{DS, Sat(mn4)} + V_{DS, Triode(mn2)} \quad 3.2$$

where $V_{DS, Sat(mn4)}$ corresponds to the minimum drain-to-source potential when mn4 is operating in saturation and $V_{DS, triode(mn2)}$ corresponds to the drain-to-source potential when mn2 is operating in the triode region (note $V_{DS, triode(mn2)} < V_{DS, Sat(mn2)}$ for a fixed drain current).

The small-signal circuit for determining the n-type BDCCM input resistance is shown in Figure 3.2. The small-signal input resistance based on Figure 3.2 can be derived as [3]

$$r_{in} = \frac{V_{TEST}}{I_{TEST}} = \left(\frac{1}{g_{mb1} + g_{ds1}} \right) + \left(\frac{1}{g_{mb3} + g_{ds3}} \right) + g_{m3} \left(\frac{1}{g_{mb1} + g_{ds1}} \right) \left(\frac{1}{g_{mb3} + g_{ds3}} \right) \quad 3.3$$

which can be simplified to

$$r_{in} \cong g_{m3} \left(\frac{1}{g_{mb1} + g_{ds1}} \right) \left(\frac{1}{g_{mb3} + g_{ds3}} \right). \quad 3.4$$

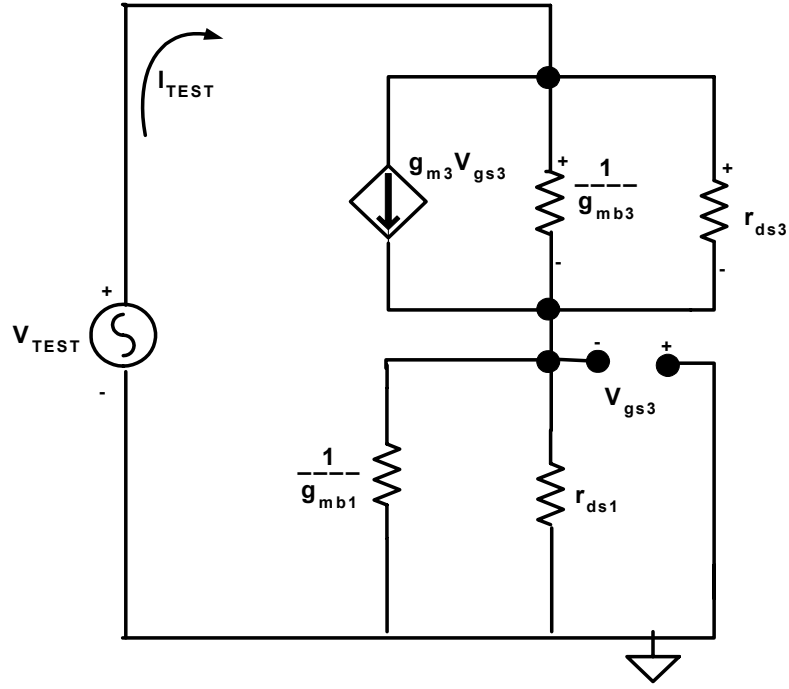


Figure 3.2: Small Signal Model NMOS BDCCM Circuit for Input Resistance.

The body-to-drain connection of transistors mn1 and mn3 forces them to operate in the triode region. This makes g_{ds1} and g_{ds3} comparable to g_{mb1} and g_{mb3} . Assuming mn1 and mn2 are perfectly matched, and that $g_m \cong \frac{1}{3}g_{mb}$, then simplifying equation (3.4) provides

$$r_{in} = g_{m3} \left(\frac{1}{4g_{mb3}} \right) = \frac{3}{4g_{mb3}} = 2.25(g_{mb3})^{-1} \quad 3.5$$

which is comparable to the gate-driven cascode current mirror small-signal input impedance that is equal to $2(g_{m3})^{-1}$ [8].

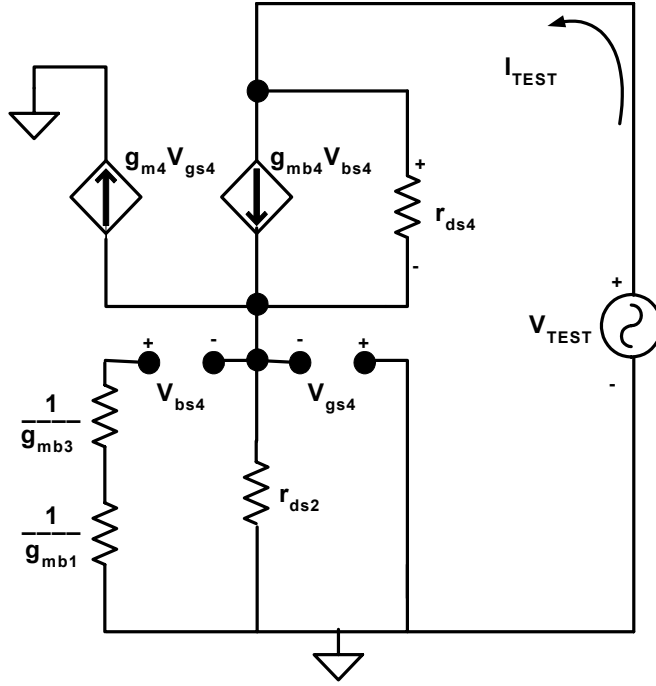


Figure 3.3: Small Signal Model NMOS BDCCM Circuit for Output Resistance.

Figure 3.3 shows the small-signal circuit for the output impedance analysis of a body-driven n-type cascode current mirror. From Figure 3.3, the output impedance can be derived as [3]

$$r_{out} = \frac{V_{TEST}}{I_{TEST}} = r_{ds2} + r_{ds4} + r_{ds4}r_{ds2}(g_{mb4} + g_{m4}) \quad 3.6$$

which simplifies to

$$r_{out} \cong r_{ds4}r_{ds2}(g_{mb4} + g_{m4}). \quad 3.7$$

Since m_{n2} is operating in the triode region, r_{ds2} is much smaller compared to r_{ds4} . The product of r_{ds2} and r_{ds4} , however, is quite large. Subsequently the output impedance r_{out} is on the order of tens to hundreds of mega-ohms. Thus, the circuit provides exceptional performance as a current mirror or current source.

3.1.2 Experimental Results for N-type BDCCM

Measurements were made on BDCCM circuits fabricated and tested in a commercial PDSOI CMOS 0.35 μ m process. Pictures of this chip, layouts, bonding diagrams, and block diagrams are included as Appendix C. Figure 3.4 shows part of the measurement procedure for the n-type BDCCM circuit using the HP4145B Semiconductor Parameter Analyzer with National Instruments Labview6 program as an interface to a laptop computer for data collection. The network connection between the HP4145B and the laptop is done using a GBIP PCMCIA network card.

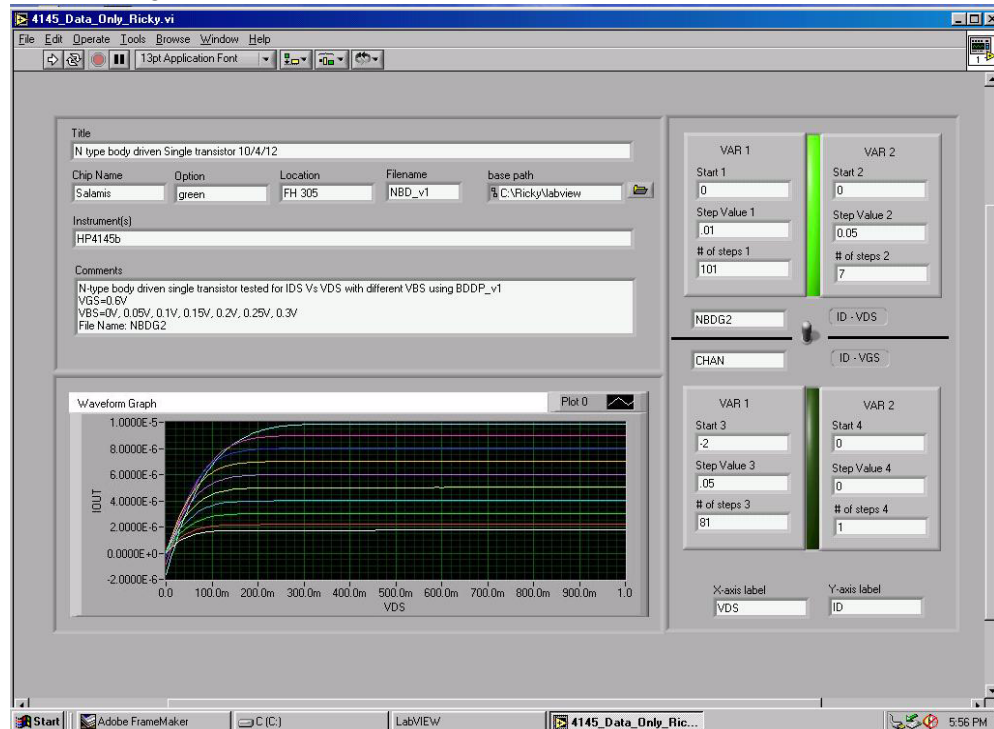


Figure 3.4: Labview6 GUI Used to Interface with HP4145B Parameter Analyzer.

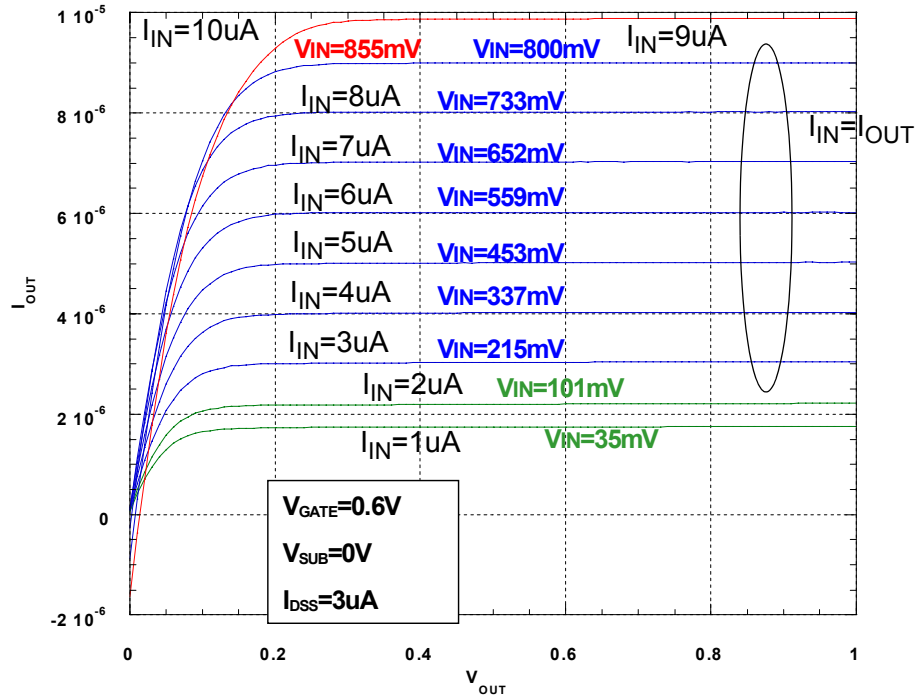


Figure 3.5: Measured Results of N-type BDCCM Circuit with Device Sizes 40/4.

Figure 3.5 shows the measured results for an n-type BDCCM with mn1-mn4 W/L of 10/4 and 4 gate fingers per transistor (total W/L ratio is 40/4 for each transistor). For this circuit, I_{OUT} and V_{IN} are measured as V_{OUT} is swept from 0V to 1V, in 20mV increments. Input current I_{IN} is increased from 1uA to 10uA with 1uA steps, and V_{GATE} is held constant at 0.6V. Simulation results of this BDCCM using Smartspice are provided in Appendix A. These simulation results show good agreement with the measured characteristics in Figure 3.5. From Figure 2.6 one can determine the I_{DSS} for this aspect ratio device and gate bias to be about 3uA. Notice that the output currents track the input currents very well from 3uA to 9uA, which is in a range of $3(I_{DSS})$. This is because when I_{IN} increases, V_{BS4} will also increase, based on equation (3.1). Once $I_{IN} > 3(I_{DSS})$, the parasitic lateral bipolar junction transistor of mn1 and mn3 will turn-on due to large V_{BS}

(which is V_{BE} of the lateral BJT) causing part of the drain current to leak to the body (the lateral BJT's base terminal). I_{OUT} will no longer match the input current when this happens. The measured minimum input voltage ranges from 215mV to 800mV and the minimum output voltage required for this current mirror is only 250mV. At 5 μ A, the measured output resistance is over 24M Ω , which is near the limit of the measurement instrumentation capability. To further demonstrate the low-voltage capability of this current mirror over a higher current range, two other sets of BDCCM with larger aspect ratios were also fabricated and measured for comparison. Table 3.1 shows the measured data for a combination of n-type BDCCMs with 3 different transistor aspect ratios. The data shows a consistent trend with a low-voltage requirement over a large range of currents. Furthermore, agreement with spice simulation within 1% for the $I_{OUT}=I_{IN}$ range is demonstrated¹. A low output voltage of no greater than 300mV and the high small-signal output resistance in the mega-ohms range make the BDCCM an excellent candidate for a wide range of analog circuits such as folded cascode gain stages and differential pair load.

Table 3.1: Measured Data for N-type BDCCM with Different Aspect Ratio.

BDCCM aspect Ratio	$I_{OUT}=I_{IN}$ Range	$I_{OUT}=I_{IN}$ Range (Spice)	V_{IN} Range	$V_{OUT,Min}$	I_{DSS}	r_{out}
NMOS 10/4/12 (W/L = 120/4)	9 μ A-28 μ A	9 μ A-30 μ A	190-774mV	~260mV	~9 μ A	>6M Ω @18 μ A
NMOS 10/4/4 (W/L = 40/4)	3 μ A-9 μ A	3 μ A-9 μ A	215-800mV	~250mV	~3 μ A	>24M Ω @5 μ A
NMOS 10/2/12 (W/L = 120/2)	20 μ A-50 μ A	18 μ A-56 μ A	232-787mV	~300mV	~18 μ A	>7M Ω @40 μ A

1. Simulation uses “typical” process corner model at room temperature.

3.1.3 Experimental Results for P-type BDCCM

Figure 3.6 shows a p-type version of BDCCM circuit block. The functionality of this circuit is similar to the n-type version, but now a sourcing current is provided. The gate terminal is common for mp1-mp4 and is biased to provide a conduction channel for each MOSFET. Here again, the body terminals are utilized to control current modulation.

To demonstrate the low-voltage capability of a p-type BDCCM, several versions of p-type BDCCM were fabricated and tested in the same process as the n-type BDCCM. Figure 3.7 shows the measured results for a p-type BDCCM with mp1-mp4 W/L of 10/4 and 4 gate fingers per transistor (again, total W/L of 40/4). I_{OUT} and V_{IN} are measured as V_{OUT} is swept from 0V to 1V, in 20mV increments, where input current I_{IN} is decreased from

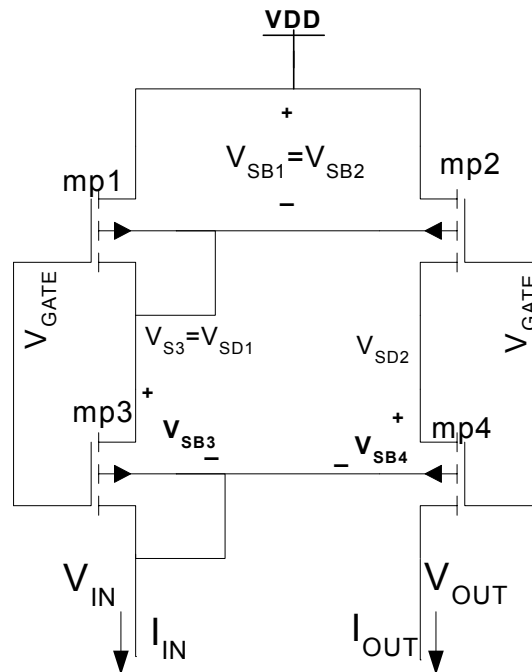


Figure 3.6: P-type BDCCM Circuit Block

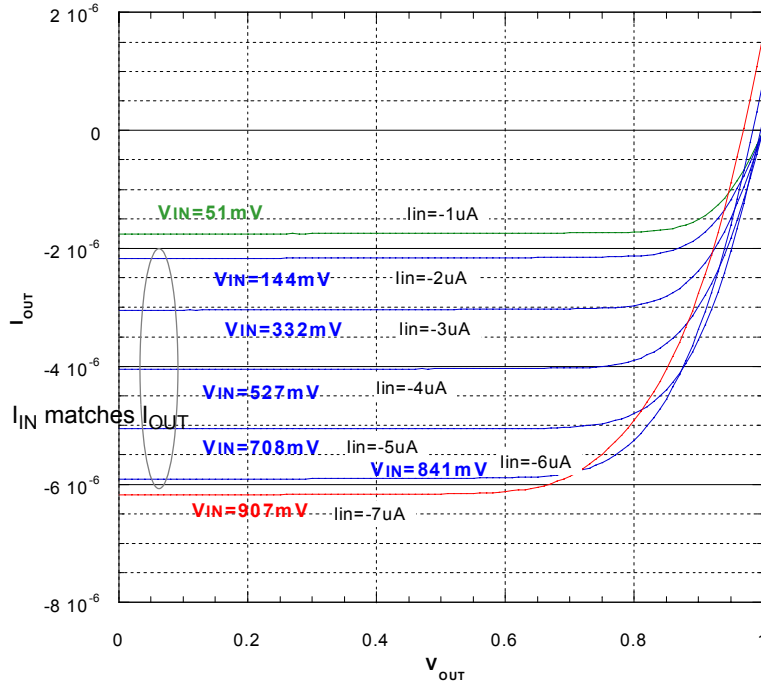


Figure 3.7: Measured Results of P-type BDCCM Circuit with Device Sizes 40/4.

-1 μ A to -7 μ A with -1 μ A steps, and V_{GATE} is held at 0V. Simulation results of this p-type BDCCM using Smartspice are also provided in Appendix A and agree well with the measured characteristics. The measured output currents track the input currents very well from -3 μ A to -6 μ A, which is in a range of $2(I_{DSS})$ where the measured I_{DSS} for this aspect ratio transistor with $V_{SG}=1$ V is shown in Figure 2.6 to be about -3 μ A. Similar to the n-type BDCCM, the parasitic lateral bipolar junction transistor associated with mp1 and mp3 will turn-on once $I_{IN} > 2(I_{DSS})$ due to large V_{SB} (since $V_{SB}=V_{EB}$ of the parasitic lateral pnp BJT). This causing part of the drain current to leak to the body (the lateral BJT's base terminal) and I_{OUT} will no longer match with the input current. The measured input voltage ranges from 332mV to 841mV and the minimum output voltage required for this current mirror is only 350mV. Table 3.2 summarizes measured data for the p-type BDCCM with transistors of 3 different aspect ratios. Simulation results are also provided

Table 3.2: Measured Data for P-type BDCCM with Different Aspect Ratio.

BDCCM aspect Ratio	$I_{OUT}=I_{IN}$ Range	$I_{OUT}=I_{IN}$ Range (Spice)	V_{IN} Range	$V_{OUT,Min}$	I_{DSS}	r_{out}
PMOS 10/4/12 (W/L = 120/4)	8 μ A-16 μ A	8 μ A-20 μ A	271-756mV	~360mV	~8.5 μ A	>7.67M Ω @12 μ A
PMOS 10/4/4 (W/L = 40/4)	3 μ A-6 μ A	3 μ A-7 μ A	332-841mV	~350mV	~3 μ A	>24.4M Ω @4 μ A
PMOS 10/2/12 (W/L = 120/2)	20 μ A-30 μ A	20 μ A-38 μ A	251-613mV	~300mV	~19 μ A	>3.07M Ω @24 μ A

in Table 3.2. The I_{DSS} in Table 3.2 is intentionally made to match with the I_{DSS} shown in Table 3.1 by careful tuning of V_{GATE} for both p-type and n-type. The data demonstrates a consistent trend with exceptional low supply voltage characteristics over a wide range of currents. The measured data agrees with spice simulation within 1% for the $I_{OUT}=I_{IN}$ matching current range¹. Highlights include low output voltage no greater than 400mV and high small-signal output resistance in the mega-ohms range. Coupled with its n-type counterpart, design of low-voltage analog systems is conceivable using BDCCMs.

3.2 Body-Driven Differential Pair (BDDP) in PDSOI

3.2.1 Theory

Differential pairs are another critical analog building block that is subject to V_{TH} limitations. The minimum supply voltage imposed by the gate-driven differential pair is equal to a threshold voltage V_{TH} plus two overdrive voltages $V_{DS,SAT}$ (assuming a single transistor tail current bias). For a typical CMOS process, this voltage requirement turns out to be around 1V. Furthermore, to widen the input common-mode range (ICMR) and

1. Simulation uses “typical” process corner model at room temperature.

reduce the transconductance variation with common-mode voltage [3], parallel connected complementary gate-driven differential pairs are often utilized. Unfortunately, conventional dual-pairs circuits [8] cannot operate below 1.5V. Early work using the body-driven technique in analog circuits in bulk CMOS [3] successfully demonstrated a body-driven differential pair for low-voltage applications, but again the technology did not permit body-driving of both p- and n-type transistors. Thus, this investigation explores complementary body-driven differential pairs (BDDPs) in PDSOI.

First consider each type of BDDP individually, beginning with the n-type version. The n-type body-driven differential pair is shown in Figure 3.8. Again, when body-driving, the gates of both mn1 and mn2 are tied to V_{GATE} to form the inversion channel beneath each transistor's gate. Since each transistor can have it's own individual body in PDSOI, a differential voltage signal can be applied between the body terminals of mn1 and mn2.

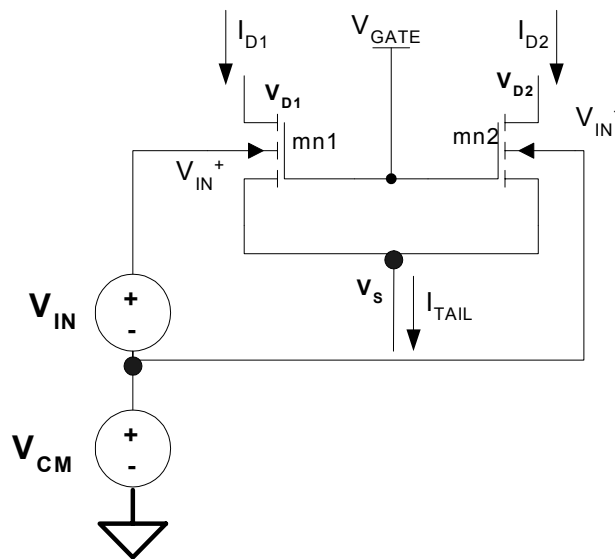


Figure 3.8: N-type BDDP Circuit Block.

This differential input signal will cause the drain current to be steered between mn1 and mn2 such that

$$I_{D1} - I_{D2} = G_{mb} V_{IN} \quad 3.8$$

where G_{mb} is the differential transconductance and V_{IN} is the differential input voltage signal [8]. The differential transconductance gain (G_{mb}) of this differential pair can be described by

$$G_{mb} = \frac{\gamma g_m}{2\sqrt{2|\phi_F| + V_{CM} - V_S}} = \frac{\gamma \sqrt{\mu_n C_{OX} \left(\frac{W}{L}\right) I_{TAIL}}}{2\sqrt{2|\phi_F| - V_{CM} + V_S}} \quad 3.9$$

where V_{CM} is the common-mode voltage at the body terminals, V_S is the source-coupled node voltage and I_{TAIL} is tail current used to bias the differential pair [3]. The BDDP will tend to provide much wider ICMR compared to the gate-driven differential pair (with respect to supply voltage) because V_{CM} applied to the BDDP can swing rail-to-rail while operating from a 1V supply. This is because the body-to-drain diode can be reversed-biased, zero-biased, or forward-biased depending on V_{CM} . In addition, when V_{CM} moves away from V_S (forward-biasing V_{BS}), the threshold voltage tends to change with the common-mode voltage due to body effect. However, since the source-coupled node is connected to a current source, V_S will somewhat track the common-mode voltage within the midrange of ICMR. Consequently, the body-to-source diode is not excessively forward-biased near a given extreme of ICMR, thus preventing the parasitic lateral BJT from turning-on and compromising input impedance [3]. Within a 1V (or lower) system,

the body terminals of the BDDP will maintain high input impedance, which is essential for proper operation within analog applications.

3.2.2 Experiment Results of N-type BDDP

Figure 3.9 shows the measured data on a n-type BDDP fabricated in a 0.35 μ m PDSOI CMOS process. The aspect ratio of both mn1 and mn2 is 40/4 (4 gate fingers, 10/4 per gate). I_{D1} and I_{D2} are measured while sweeping V_{in}^+ from -0.3V to 0.3V and V_{in}^- from 0.3V to -0.3V (simultaneously) per I_{Tail} step of 2 μ A to 10 μ A in 2 μ A increments. V_{D1} and V_{D2} are both connected to 0.2V and V_{GATE} is connected to 0.5V. A voltage compliance limit established for V_S prevents the source-coupled node from going below -0.3V during the measurement. These voltages were carefully selected to establish V_{CM} equal to 0V when V_{DD} and V_{SS} are 0.5V to -0.5V, respectively. The simulation results (see Appendix A) agree nicely with measured data. This comparison is described quantitatively in Table 3.3 for a I_{Tail} of 6 μ A. To demonstrate the operation of the BDDP over a wider range of currents, two other versions of n-type BDDPs with aspect ratio of 10/4/12 (total W/L of 120/4) and 10/2/12 (total W/L of 120/2) were also fabricated and tested. These measured results are found in Appendix B. The maximum slope of each curve in Figure 3.9 is the transconductance of BDDP (G_{mb}) for a given I_{Tail} and V_{CM} . Measured G_{mb} over the entire rail-to-rail ICMR is provided in Figure 3.10. This figure shows the change in G_{mb} with V_{CM} as I_{Tail} increases from 1 μ A to 10 μ A. For I_{Tail} =1 μ A, the measured G_{mb} increases 29.5% over the V_{CM} range of 0V to 0.5V, and decreases 9.7% over the V_{CM} range of 0V to -0.5V. For I_{Tail} =10 μ A, G_{mb} increases 27.7% over the V_{CM} range of 0V to 0.5V, and decreases 14% over the V_{CM} range of 0V to -0.5V.

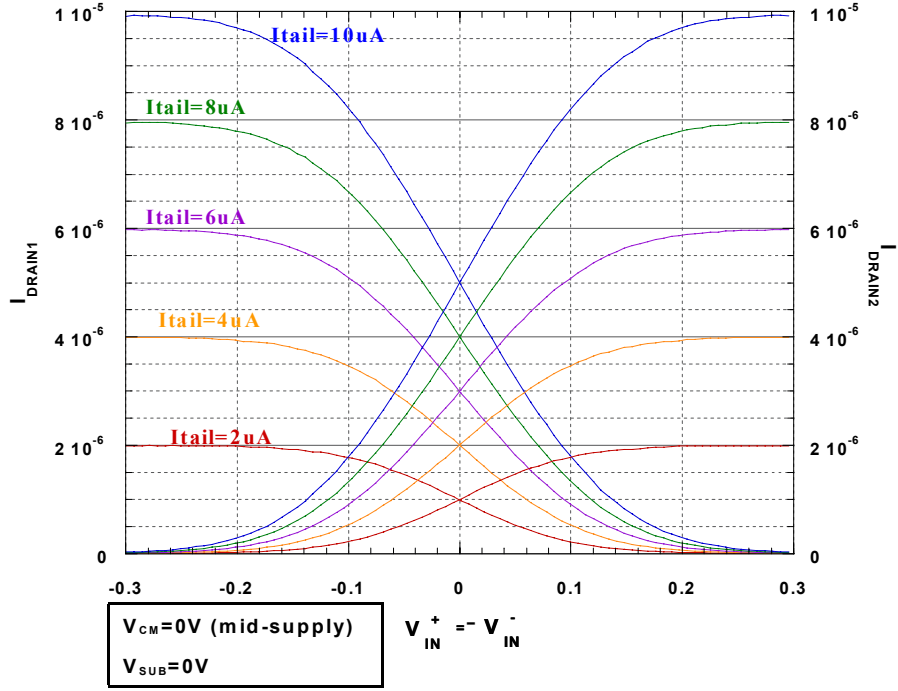


Figure 3.9: N-type BBDP Circuit with Aspect Ratio 40/4.

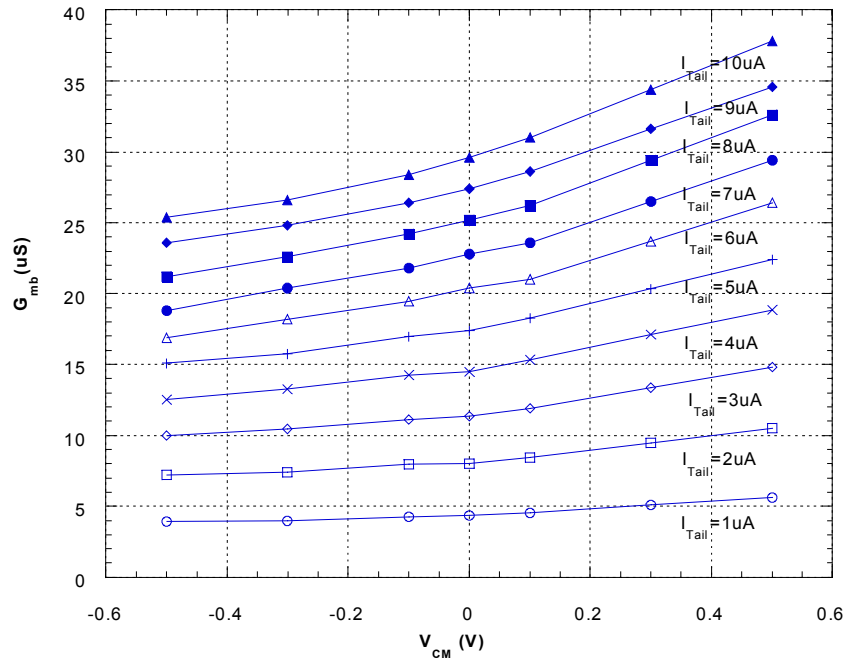


Figure 3.10: Measured G_{mb} Plot for N-type BBDP Circuit with Aspect Ratio 40/4.

3.2.3 Experiment Results of P-type BDDP

Figure 3.11 shows the measured data on a p-type BDDP with aspect ratio of 10/4 with 4 gate fingers. I_{D1} and I_{D2} are measured also by sweeping V_{in}^+ from -0.3V to 0.3V and V_{in}^- from 0.3V to -0.3V (simultaneously). I_{Tail} is swept from -2 μ A to -10 μ A with -2 μ A steps with V_{D1} and V_{D2} both connected to -0.2V and V_{GATE} is connected to -0.5V. These voltages were again carefully selected by assuming V_{CM} is equal to 0V (mid-supply) for $V_{DD}=+0.5V$ and $V_{SS}=-0.5V$. The simulation results show good agreement to measure data and are included in Appendix A. This comparison is describe quantitatively in Table 3.3 for a I_{Tail} of -9 μ A. To demonstrate the operation of BDDP over a wider range of current, two other versions of p-type BDDP with aspect ratio of 10/4/12 and 10/2/12 were also fabricated and tested. This measured data are attached as Appendix B.

Figure 3.12 shows how the p-type BDDP measured G_{mb} varies with rail-to-rail V_{CM} for different tail currents. For $I_{Tail}=-1\mu A$, the measured G_{mb} decreases 20.5% over the V_{CM} range of 0V to 0.5V, and increases 53.4% over the V_{CM} range of 0V to -0.5V. For $I_{Tail}=-10\mu A$, the measured G_{mb} decreases 24.5% over the V_{CM} range of 0V to 0.5V, and increases 41.7% over the V_{CM} range of 0V to -0.5V. These percentages are significant, but using a complementary form of the BDDP can reduce the total G_{mb} variation. Such a circuit will be described in the next section. Overall, the measured results demonstrate the low-voltage capability of BDDP (both n-type and p-type) in PDSOI.

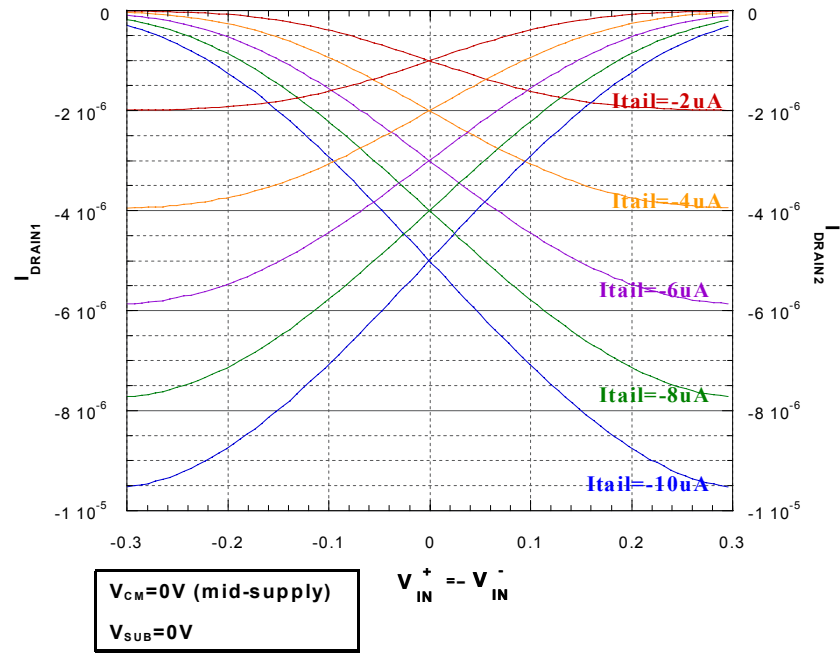


Figure 3.11: P-type BDDP Circuit with Aspect Ratio 40/4.

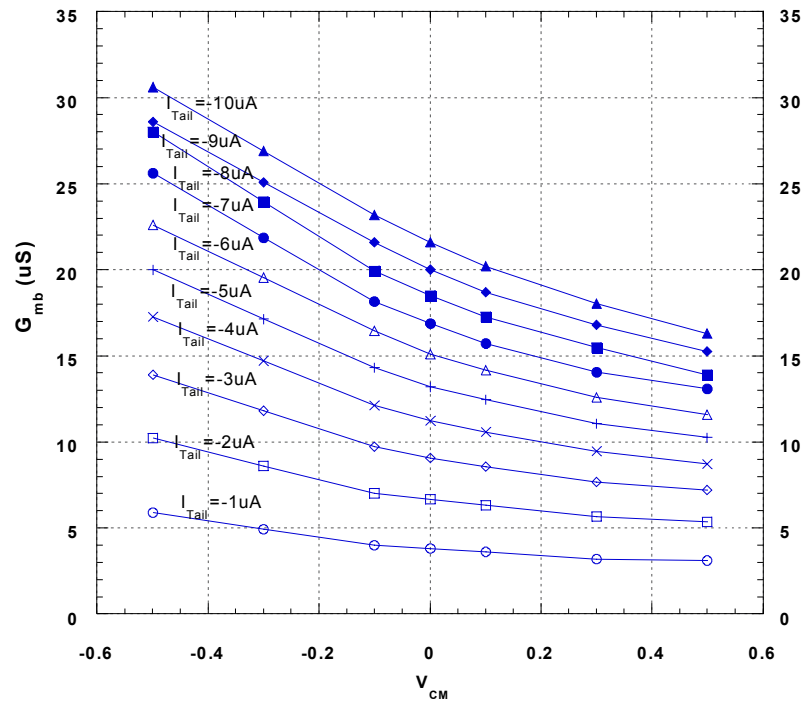


Figure 3.12: Measured G_{mb} Plot for P-type BDDP Circuit with Aspect Ratio 40/4.

3.2.4 Rail-To-Rail Constant G_{mb} Differential Input Amplifier

To maintain constant bandwidth within a multistage amplifier, the differential pair input stage must provide constant transconductance over ICMR [8]. Figure 3.13 shows a constant G_{mb} fully differential input stage with a rail-to-rail input common-mode range using complementary BDDP. This circuit is capable of 1V operation. V_{bias1} and V_{bias2} are used to set the tail current for the n-type BDDP and the p-type BDDP. The drain currents are then summed together. G_{mb} will be combined within the input stage to reduce the total variation in transconductance with V_{CM} over the rail-to-rail ICMR.

Figures 3.10 and 3.12 have shown the overall transconductance variation is much different for the n-type BDDP and the p-type BDDP. Through careful selection of tail current bias for each BDDP, the combined overall transconductance variation is minimized. Table 3.3 summaries the measured and spice simulation results of the G_{mb} percentage variation using p-type BDDP with $-9\mu A$ and n-type BDDP with $6\mu A$ and same

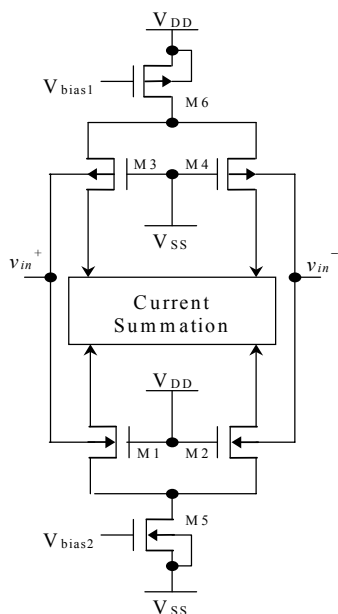


Figure 3.13: Constant G_{mb} with Complementary BDDP Input Stage.

transistor aspect ratio of 40/4. Note that the measured maximum percentage deviation for combined G_{mb} is very close to the spice simulation result. Figure 3.14 shows the combined G_{mb} variation characteristic using p-type BDDP with $-9\mu\text{A}$ tail current and n-type BDDP with $6\mu\text{A}$ tail current. Based on a literature survey, a input stage circuit with transconductance variation of less than 20% can be considered a “constant” G_m circuit. Here, the combined G_{mb} has a nominal value of $41.7\mu\text{S}$ (at $V_{CM}=0\text{V}$) and a maximum variation of only 9.04% from the nominal. This is a tremendous improvement from the percentage variation demonstrated by the individual n-type and p-type BDDPs over rail-to-rail V_{CM} of 1V as shown in Table 3.3.

Having discussed both BDDP and BDCCM circuits, one should recognize that the p-type BDCCM could readily be used to load an n-type BDDP, or vice-versa, to form an operational transconductance amplifier (OTA). Furthermore, by combining complementary versions of such an amplifier, the resultant circuit could take full advantage of the constant- G_{mb} over rail-to-rail ICMR provided by complementary BDDPs. .

Table 3.3: Summary of Constant G_{mb} Differential Input Amplifier

	Measured vs. (Spice) G_{mb} % variation for $V_{CM}=-0.5\text{V}$ to 0V	Measured vs. (Spice) G_{mb} % variation for $V_{CM}=0\text{V}$ to 0.5V	Max % Deviation For Combined G_{mb} from $V_{CM}=0\text{V}$	Max % Deviation For Combined G_{mb} from $V_{CM}=0\text{V}$ (Spice)
N-type BDDP ($I_{tail}=6\mu\text{A}$)	17% (11.1%)	29.4% (23.2%)	9.04%	8.05%
P-type BDDP ($I_{tail}=-9\mu\text{A}$)	51.2% (47.7%)	25% (23.4%)		

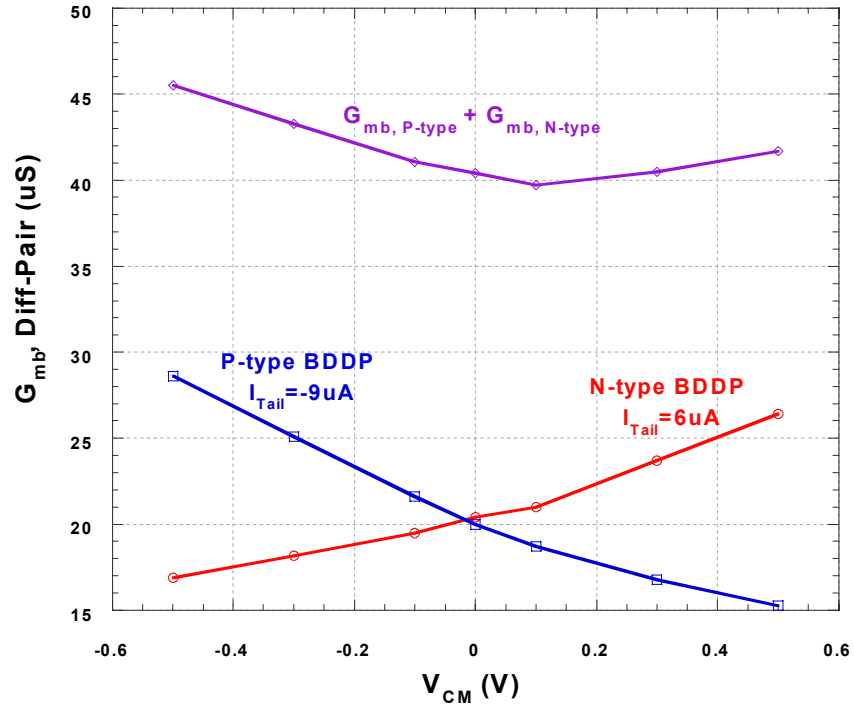


Figure 3.14: Measured Data of Constant G_{mb} Differential Input Amplifier.

3.3 Body-Driven 4-Quadrant Analog Multiplier (BDAM)

3.3.1 Theory

A 4-quadrant multiplier capable of operating from low supply voltage is a valuable building block for analog signal processing, particularly communication applications. Previous work on a 4-quadrant analog multiplier using body-driving techniques in a $0.5\mu m$ bulk CMOS process successfully demonstrated modulation of a 1MHz, $100mV_{p-p}$ sine wave signal by a 10MHz carrier signal during 1.2V operation [13]. Unfortunately, this BDAM has limited frequency capability due to large input capacitance attributed to body-driving in bulk CMOS. In addition, only the p-type BDAM can be implemented in a n-well bulk CMOS technology. Thus, this work explores the BDAM circuit in PDSOI technology to provide both p-type and n-type versions. This should also reduce the input

capacitance penalty when the transistors are body-driven. Figure 3.15 shows the schematic of a p-type body-driven 4-quadrant analog multiplier core. The circuit utilizes both the gate and body terminals of the transistors to perform current modulation using a minimum number of transistors. Transistors m1-m4 are identically sized for optimal matching. Inspection of the BDAM circuit reveals that $V_{SG1}=V_{SG2}$, $V_{SG3}=V_{SG4}$, $V_{SB1}=V_{SB2}$, and $V_{SB3}=V_{SB4}$. The differential output current I_{Diff} of the BDAM can be described as

$$I_{Diff} = (i_1 + i_3) - (i_2 + i_4) = (i_1 - i_2) + (i_3 - i_4). \quad 3.10$$

Since

$$V_{in1} = V_{SB2} - V_{SB1} = V_{SB3} - V_{SB4} \quad 3.11$$

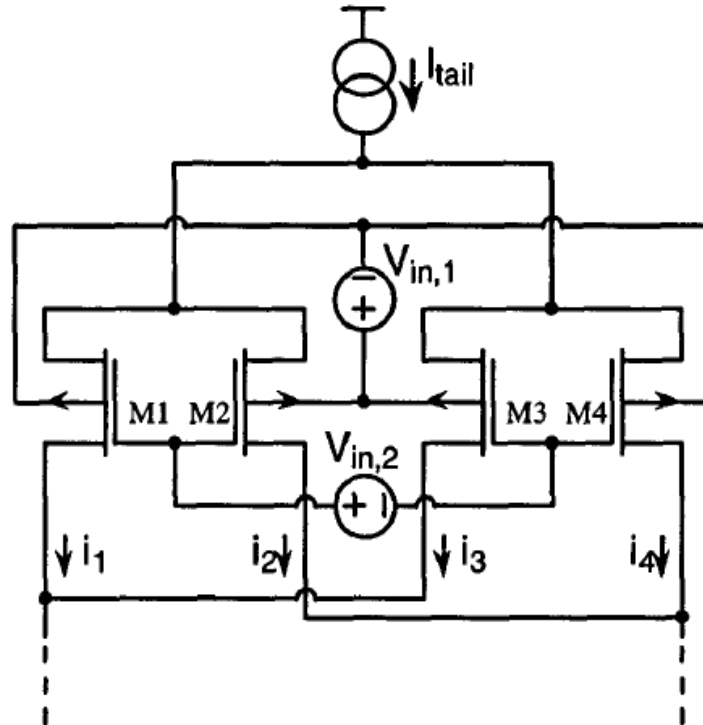


Figure 3.15: Schematic of 4-Quadrant Multiplier with 4 Transistor [13].

and

$$V_{in2} = V_{SG1} - V_{SG3} = V_{SG2} - V_{SG4}, \quad 3.12$$

then using the MOSFET square-law relationship provides an expression for I_{Diff} that reduces to [13]

$$I_{Diff} = K'_p \left(\frac{\gamma_p}{\sqrt{2}|\phi_F|} \right) (V_{in1} V_{in2}). \quad 3.13$$

This equation describes the 4-quadrant linear multiplication of two analog signals input to this circuit.

3.3.2 Experiment Results of N-type BDAM

Measured results for a n-type BDAM circuit fabricated on a 0.35 μ m PDSOI process is shown in Figure 3.16. Again, this circuit is only possible in PDSOI technology. A supply

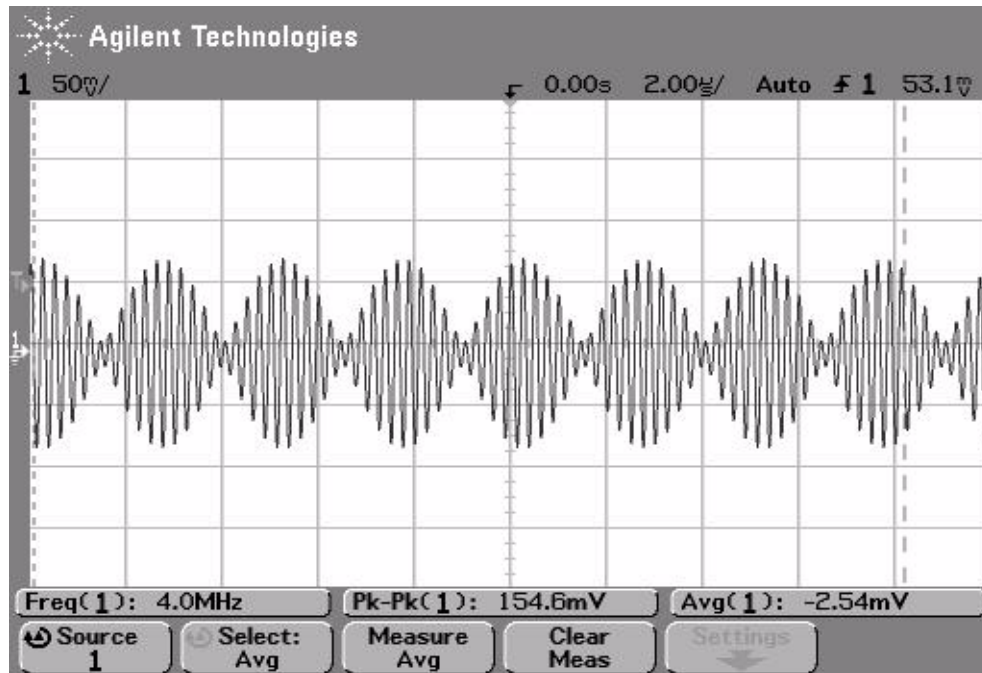


Figure 3.16: Agilent 54622D Oscilloscope Plot for N-type BDAM

voltage of 1.0V and tail current of 166 μ A is used during the measurements. Linear mixing of a 150mV_{p-p}, 200kHz signal (V_{IN1}) with a 120mV_{p-p}, 4MHz carrier signal (V_{IN2}) is achieved. Higher frequency signals are not demonstrated because of the 8MHz gain-bandwidth limitation of the MC34081 operational amplifier used on the test board. The schematic and photograph of the test board used for this measurement are included in Appendix C. The simulated result, which agrees with Figure 3.16, is included as Appendix B. Figure 3.17 shows the frequency spectrum generated by the n-type BDAM when performing linear amplitude modulation to achieve Double Side Band Suppressed Carrier (DSBSC) measured using the HP8590L Spectrum Analyzer. Note that carrier feed-through at 4MHz is suppressed approximately 50dB below the modulated input, likely due to coupling on the test board. As expected, the side-band bandwidth is approximately 400kHz. The third and higher harmonics are barely noticeable in Figure 3.17. Hence, this multiplier has demonstrated amplitude modulation with relatively low distortion and low supply voltage (1V). Overall, these results imply that the BDAM in PDSOI can readily provide mixing capability for IF (Intermediate Frequency) in low voltage communication systems.

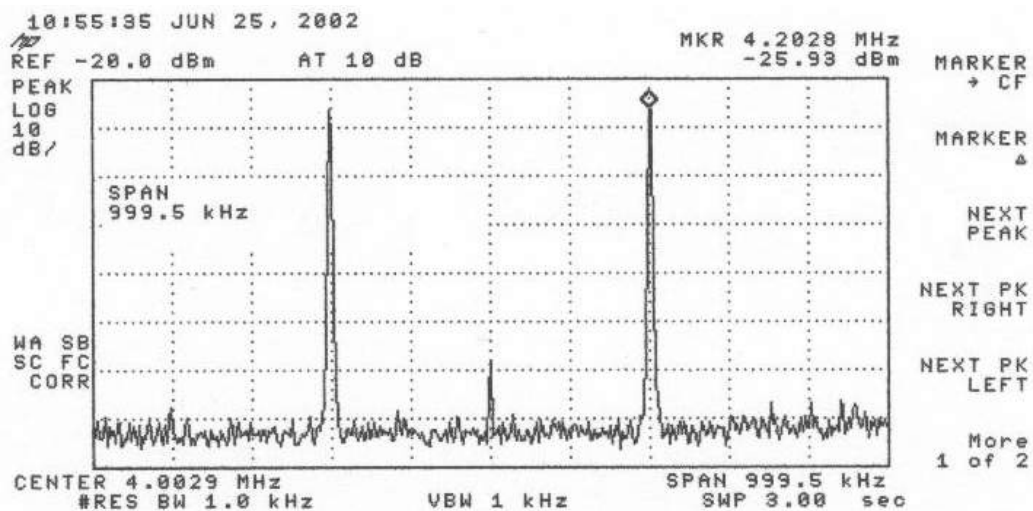


Figure 3.17: HP8590L Spectrum Analyzer Plot for N-type BDAM.

Chapter 4

Conclusions and Future Improvements

A brief survey of analog applications for the body-driving technique in partially-depleted SOI technology has been provided. Specific design issues related to several body-driven analog circuits have been analyzed and discussed in detail. Layout techniques and test results of prototype circuits were presented. This chapter summarizes the prototype measurements and discusses ideas for future work utilizing the body-driven circuit design technique.

4.1 Conclusions

Several body-driven analog circuit building block primitives were fabricated on a 3.3V PDSOI 0.35 μ m process. Measurements of the prototype circuits are in agreement with the expected results from Spice simulation. It has been shown that SOI is an ideal vehicle for body-driven circuits because each device can have a unique body terminal. The circuits presented were capable of operating at a very low voltage (1V), even with 0.6V and -0.9V threshold voltages for the NMOS and PMOS, respectively. Body-driving in PDSOI has also shown to have at least 3 times smaller input capacitance penalty compared to body-driving in bulk CMOS. Hence, body-driven circuits in PDSOI will have better high frequency performance than body-driven circuits developed in bulk CMOS.

The body-driven cascode current mirror demonstrated a very promising high output impedance for low voltage applications. As a whole, the BDCCM performance is fairly

consistent with expectations compared with Spice simulations. Both the BDDP and BDAM performed very well and were also consistent with predictions from computer simulations using Smartspice. This implies that the same spice model used for gate-driven circuits can also be used to design body-driven circuits.

4.2 Future Work

As mentioned previously in Chapter 3, one immediate suggestion for future work is utilizing the BDCCM to load a BDDP to provide a 1V capable OTA. In addition, since complementary body-driven circuits are viable in PDSOI, then complementary 1V OTAs can be combined to provide constant-G_m over rail-to-rail ICMR. Using this circuit as an input stage followed by a power efficient class-AB 1V output stage, a rail-to-rail input/output op amp in PDSOI is conceivable. Such an op amp would be a valuable asset to 1V analog signal processing systems. To realize this op amp, however, additional research is needed to develop 1V capable class-AB output stage circuits. Note also that 1V capable biasing/reference circuits are required to enable standalone analog circuit cells that need only be connected to the supply voltage to properly bias themselves.

To the best of our knowledge, this work provides the first demonstration of analog complementary body-driven circuits. Overall, the body-driving techniques in PDSOI and prototype circuits presented in this thesis have established a solid, working foundation for the development and implementation of ultra low voltage analog systems in the future.

References

1. B. J. Blalock, "Body-driving As A Low-Voltage Analog Design Technique For CMOS Technology," invited paper in the *Proceedings of the 2000 Midwest Symposium on Mixed-Signal Design*, 2000, pp.113-118.
2. Takayasu Sakurai, "Low-power And High-Speed VLSI Design With Low Supply Voltage Through Cooperation Between Levels," *Proceeding of the International Symposium on Quality Electronic Design (ISQED'02)* 2002.
3. B.J Blalock, "A 1-Volt CMOS Wide Dynamic Range Operation Amplifier," (Ph.D. Dissertation, Dept. of ECE, Georgia Institute of Technology, Georgia, GA, 1996).
4. B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V Op Amps using Standard Digital CMOS Technology," *IEEE Trans. on Circuits and Systems II*, vol. 45, no. 7, pp. 769-780, July 1998.
5. P. E. Allen, B. J. Blalock, and G. A. Rincon, "A 1-Volt CMOS Op Amp Using Bulk-Driven MOSFETs," in *Dig. 1995 IEEE Int. Solid-State Circuits Conf.*, Feb. 1995, pp. 192-193.
6. D.A. Johns and K. Martin, "Analog Integrated Circuit Design," John Wiley and Sons, New York, 1997.
7. Semiconductor Industry Association (SIA), "International Roadmap for Semiconductors 2001 Edition," International SEMATECH, 2002, Available at <http://public.itrs.net>, Austin, TX.
8. R. Jacob Baker, Harry W. Li, David E. Boyce, "CMOS Circuit Design, Layout, and Simulation," John Willey and Sons, New York, 1998.
9. Kerry Bernstein, Norman J. Rohrer, "SOI Circuit Design Concepts," Kluwer Academic Publishers, Norwell, 2000.
10. Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits," Cambridge University Press, New York, 1998.
11. Behzad Rezavi, RF Microelectronics, Prentice Hall, 1998.

12. Bernard Sklar, Digital Communications: Fundamentals and Applications, Prentice Hall, 1988.
13. Benjamin J. Blalock, Scott A. Jackson, "A 1.2V CMOS Four-Quadrant Analog Multiplier," in Proc. 1999 Southwest Symp. on Mixed-Signal Design, 1999, pp. 1-4
14. Paul R. Gray and Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley & Sons, 1993.
15. Software Application: HSPICE, Version 98.2 (980711), Avant! Corporation, 1985-1997
16. Software Application: SmartSPICE, Version 1.9.4.R, Silvaco International, 1987-2001
17. Software Application: CADENCE Version 4.4.6.100.29, Cadence Design System Inc. 2001.
18. Software Library: ITD/AuE Standard-cell Library, Microsystems Processing Laboratory, Mississippi State University, 1995-1998.
19. Benjamin J. Blalock, Personal communication, 1999-2002.

Appendices

Appendix A: Smartspice Simulation Files and Results

A.1: N-type BDCCM Simulation File and Results

```

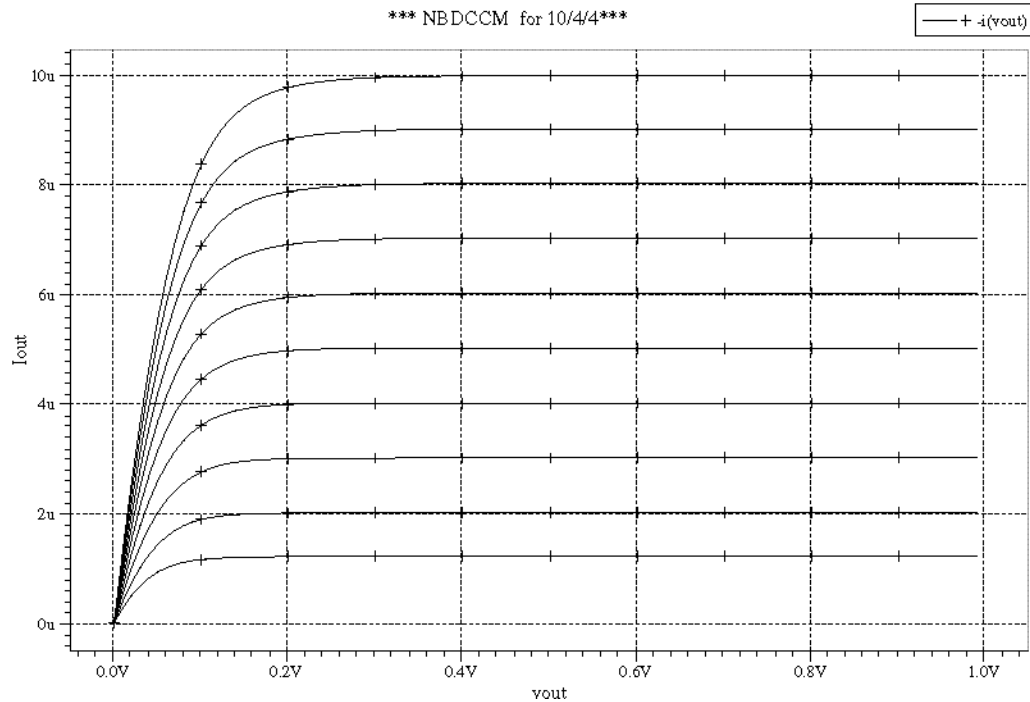
*** NBDCCM ***
*w=10 l=4

.options post ingold=2 tnom=27 nomod
.op
.dc lin vout 0 1 10m iin 1u 10u 1u
.param vssr=0.0 vccr=1
.param lay_lam=1u mw1=10 ml1=4
v_vdd vdd 0 vccr
v_vss vss 0 vssr
vgate gate 0 0.65
iin vdd 1 1u
vout 4 vss 0
*vmiin 5 1 0
*
m1 1 gate 2 1 N w='mw1*lay_lam' l='ml1*lay_lam' m=4
*+ ad='mw1*lay_lam*5*lay_lam' as='mw1*lay_lam*5*lay_lam'
*+ pd='2*mw1*lay_lam+2*5*lay_lam' ps='2*mw1*lay_lam+2*5*lay_lam'
m2 2 gate vss 2 N w='mw1*lay_lam' l='ml1*lay_lam' m=4
*+ ad='mw1*lay_lam*5*lay_lam' as='mw1*lay_lam*5*lay_lam'
*+ pd='2*mw1*lay_lam+2*5*lay_lam' ps='2*mw1*lay_lam+2*5*lay_lam'
m3 4 gate 3 1 N w='mw1*lay_lam' l='ml1*lay_lam' m=4
*+ ad='mw1*lay_lam*5*lay_lam' as='mw1*lay_lam*5*lay_lam'
*+ pd='2*mw1*lay_lam+2*5*lay_lam' ps='2*mw1*lay_lam+2*5*lay_lam'
m4 3 gate vss 2 N w='mw1*lay_lam' l='ml1*lay_lam' m=4
*+ ad='mw1*lay_lam*5*lay_lam' as='mw1*lay_lam*5*lay_lam'
*+ pd='2*mw1*lay_lam+2*5*lay_lam' ps='2*mw1*lay_lam+2*5*lay_lam'
*
.include './tt.mod'
.end

```

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Sun Jun 23 11:27 2002



A.2: P-type BDCCM Smartspice Input File and Result

```

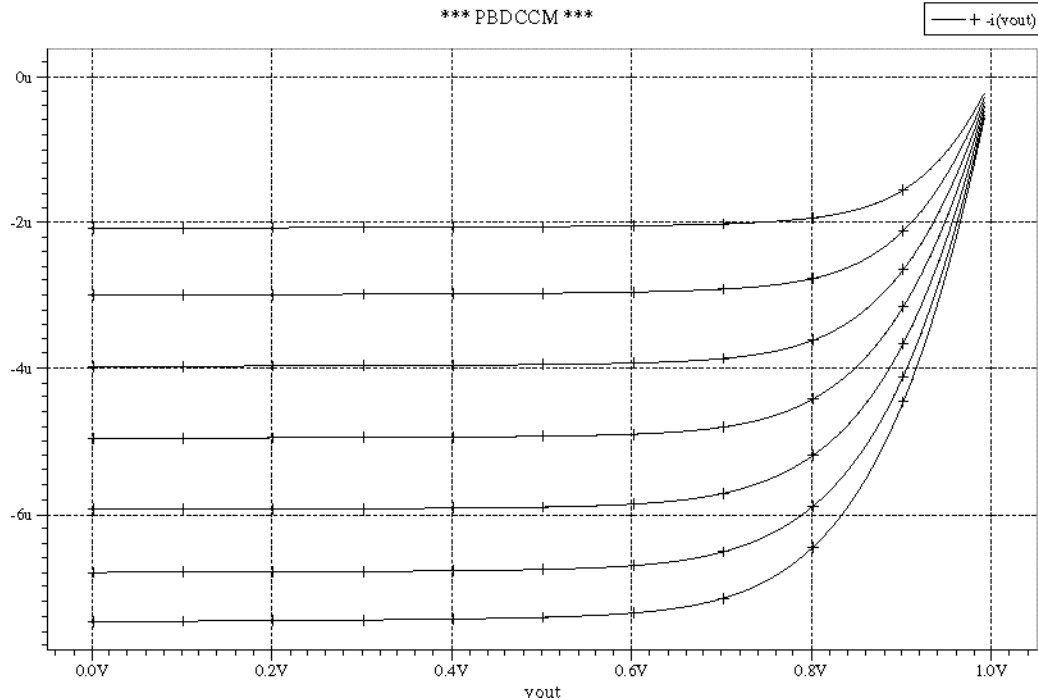
*** PBDCCM ***
*w=10 l=4 m=4

.options post ingold=2 tn timer=27 nomod
.op
.dc lin vout 0 1 10m iin -2u -8u -1u
.param vssr=0.0 vccr=1
.param lay_lam=1u mw1=10 ml1=4
v_vdd vdd 0 vccr
v_vss vss 0 vssr
vgate gate 0 0
iin vdd 5 -1u
vout 4 vss 0
vmin 1 5 0
*
m1 1 gate 2 1 P w='mw1*lay_lam' l='ml1*lay_lam' m=4
*+ ad='mw1*lay_lam*5*lay_lam' as='mw1*lay_lam*5*lay_lam'
*+ pd='2*mw1*lay_lam+2*5*lay_lam' ps='2*mw1*lay_lam+2*5*lay_lam'
m2 2 gate vdd 2 P w='mw1*lay_lam' l='ml1*lay_lam' m=4
*+ ad='mw1*lay_lam*5*lay_lam' as='mw1*lay_lam*5*lay_lam'
*+ pd='2*mw1*lay_lam+2*5*lay_lam' ps='2*mw1*lay_lam+2*5*lay_lam'
m3 4 gate 3 1 P w='mw1*lay_lam' l='ml1*lay_lam' m=4
*+ ad='mw1*lay_lam*5*lay_lam' as='mw1*lay_lam*5*lay_lam'
*+ pd='2*mw1*lay_lam+2*5*lay_lam' ps='2*mw1*lay_lam+2*5*lay_lam'
m4 3 gate vdd 2 P w='mw1*lay_lam' l='ml1*lay_lam' m=4
*+ ad='mw1*lay_lam*5*lay_lam' as='mw1*lay_lam*5*lay_lam'
*+ pd='2*mw1*lay_lam+2*5*lay_lam' ps='2*mw1*lay_lam+2*5*lay_lam'
*
.include './tt.mod'
.end

```

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Sun Jun 23 11:31 2002



A.3: N-type BDDP Simulation Command File and Result

```

N-type Body Driven Differential Pair 10/4/4

.OP
.INC /home/yong/simulation/models/tt.mod

.options ABSTOL=1mA VNTOL=100mV RELTOL=0.1

*.AC DEC 100 10 100X

*VDD VDD 0 1
VSS VSS 0 -0.5

M1 drain1 gate tail body1 N w=10u l=4u m=4
M2 drain2 gate tail body2 N w=10u l=4u m=4

Ibias tail VSS dc 5u
Vin body1 bcommon dc 0 ac 1
Ebody bcommon body2 body1 bcommon 1
Vb bcommon 0 0

Vg gate 0 1

Vd1 drain1 0 1
Vd2 drain2 0 1

*.tran 10e-9 0.01m 0 2e-9

.dc Vin -0.3 0.3 0.01 Ibias 1u 10u 1u

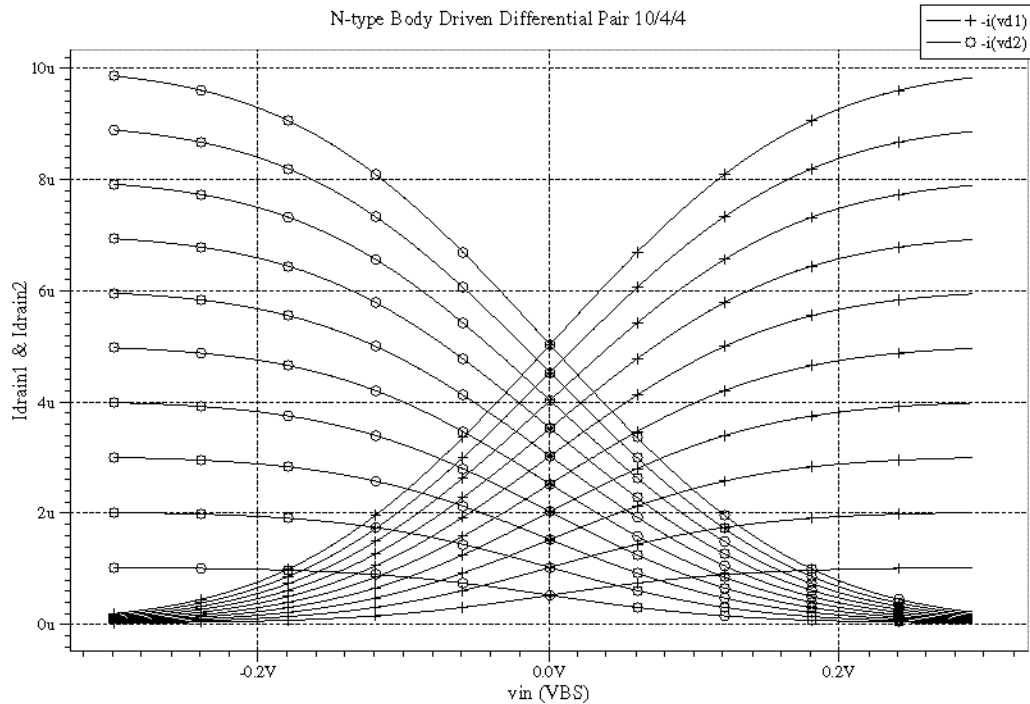
.probe v(Vin)
.probe V(Vg)
.probe V(Vb)
.probe i(Vd1)
.probe i(Vd2)

.END

```

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A.4: P-type BDDP Simulation Command File and Result

P-type Body Driven Differential Pair 10/4/4

```
.OP
.INC /home/yong/simulation/models/tt.mod

.options ABSTOL=1mA VNTOL=100mV RELTOL=0.1

*.AC DEC 100 10 100X

VDD VDD 0 0.5
VSS VSS 0 -0.5

M1 drain1 gate tail body1 P w=10u l=4u m=4
M2 drain2 gate tail body2 P w=10u l=4u m=4

Ibias VDD tail dc -5u
Vin body1 bcommon dc 1
Ebody bcommon body2 body1 bcommon 1
Vb bcommon 0 0

Vg gate 0 -0.5

Vd1 drain1 0 -0
Vd2 drain2 0 -0
*.tran 10e-9 0.01m 0 2e-9

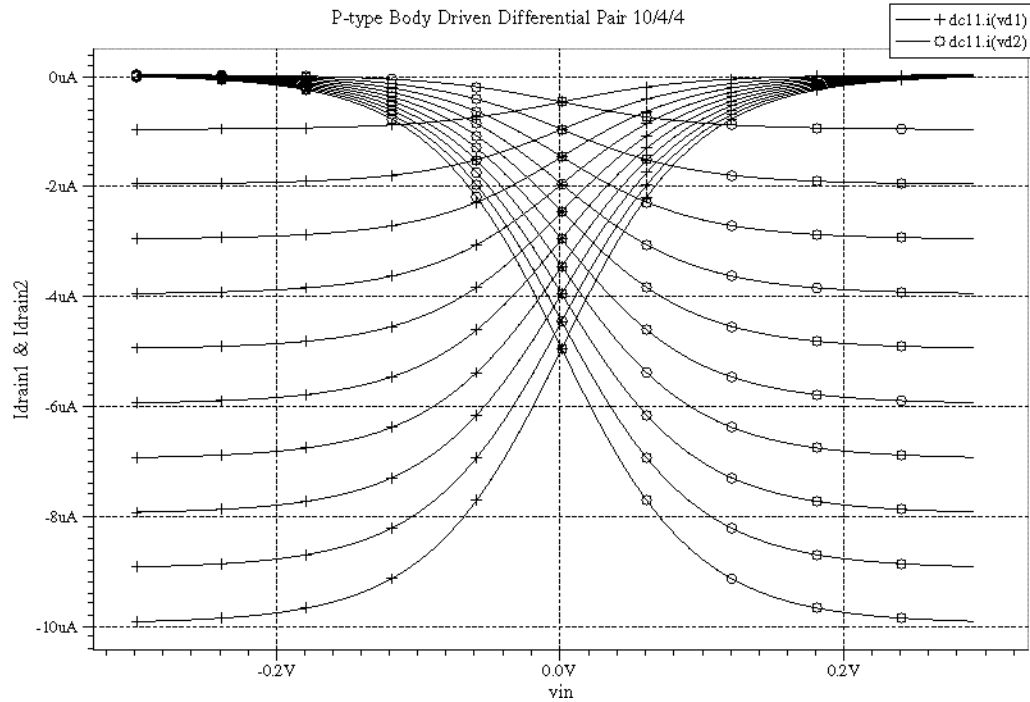
.dc Vin -0.3 0.3 0.01 Ibias -1u -10u -1u

.probe v(Vin)
.probe V(Vg)
.probe V(Vb)
.probe i(Vd1)
.probe i(Vd2)

.END
```

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A.5: N-type BADM Simulation Command File and Result

```
Body Driven 4 quadrant analog multiplier 10/4/4

.OP
.INC /home/yong/simulation/models/tt.mod

.options ABSTOL=1mA VNTOL=100mV RELTOL=0.1

*.AC DEC 100 10 100X

VDD VDD 0 1
VSS VSS 0 0

M1 drain1 gate12 tail body14 N w=10u l=4u m=4
M2 drain2 gate12 tail body23 N w=10u l=4u m=4
M3 drain3 gate34 tail body23 N w=10u l=4u m=4
M4 drain4 gate34 tail body14 N w=10u l=4u m=4

Ibias tail VSS dc 150u
Vin1 body23 bcommon dc 0 sin( 0 100e-3 200k 0 0 0)
Ebody bcommon body14 body23 bcommon 1
Vb bcommon 0 0.5

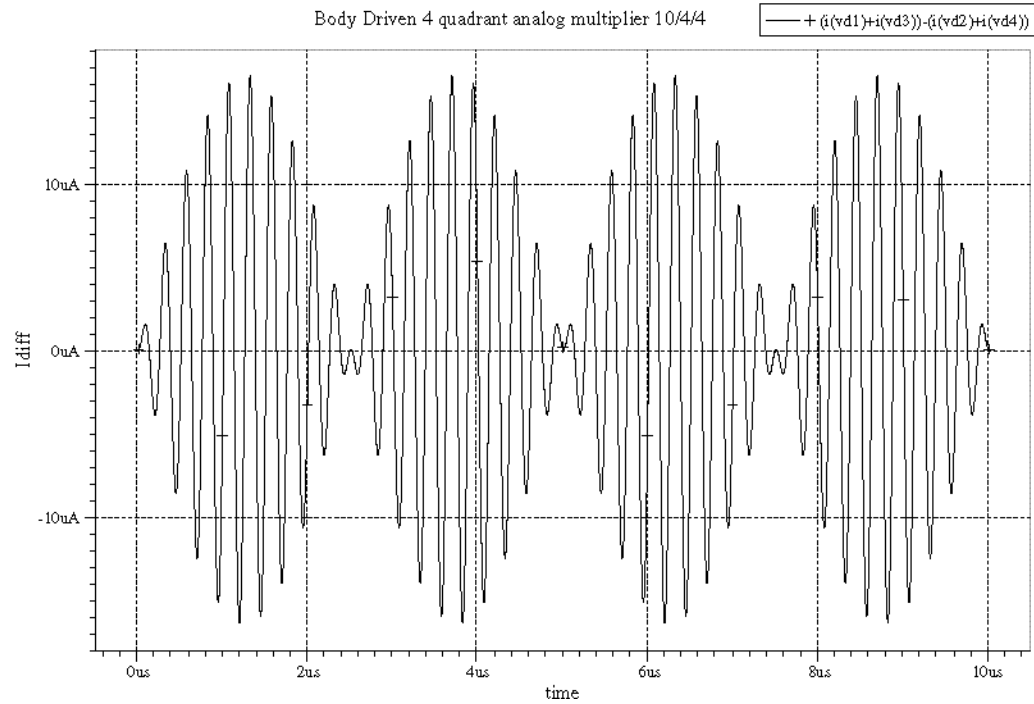
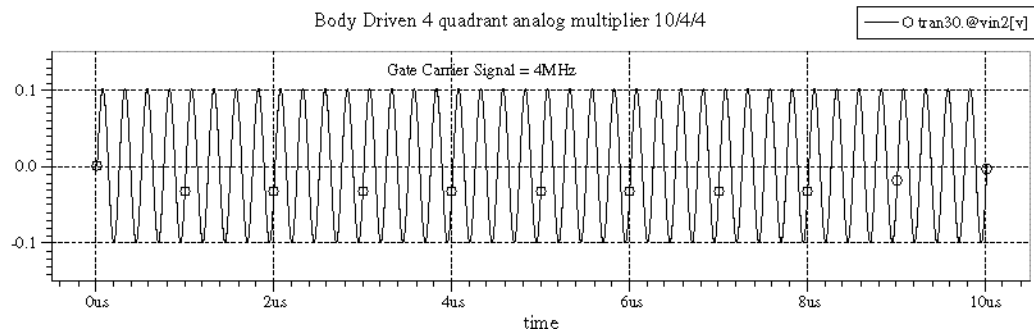
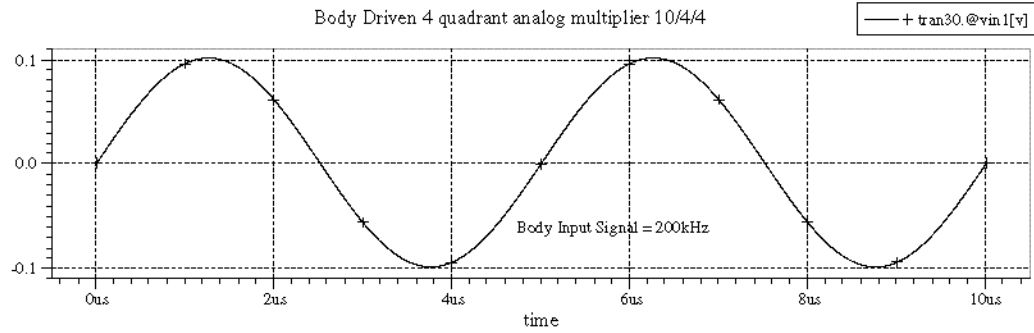
Vin2
gate12 gcommon dc 0 sin( 0 100e-3 4meg 0 0 0)
Egate gcommon gate34 gate12 gcommon 1
Vg gcommon 0 1.5

Vd1 drain1 0 2
Vd2 drain2 0 2
Vd3 drain3 0 2
Vd4 drain4 0 2

.tran 10e-9 0.01m 0 2e-9

.probe v(Vin1)
.probe v(Vin2)
.probe V(Vg)
.probe V(Vb)
.probe i(Vd1)
.probe i(Vd2)
.probe i(Vd3)
.probe i(Vd4)

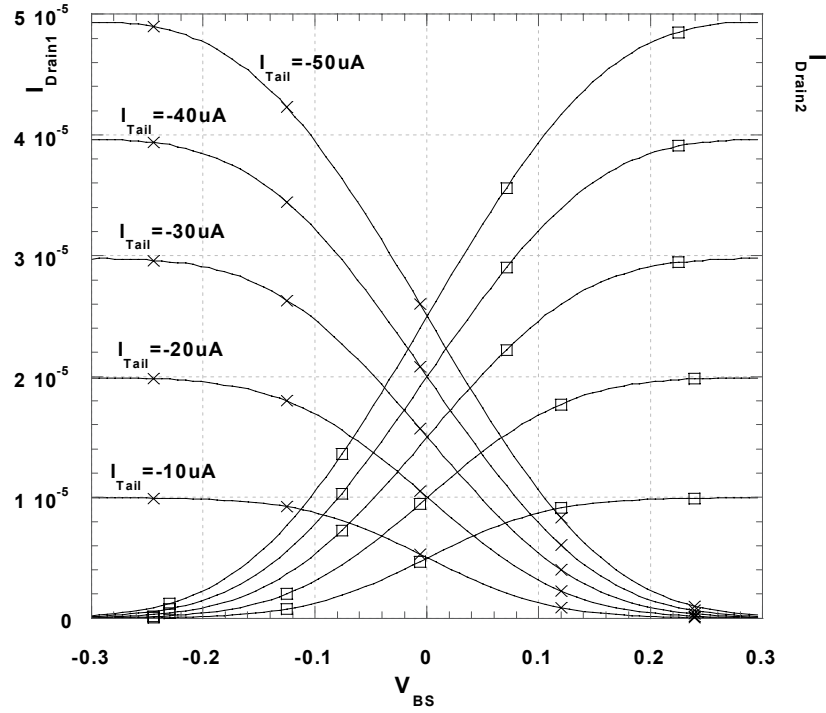
.END
```



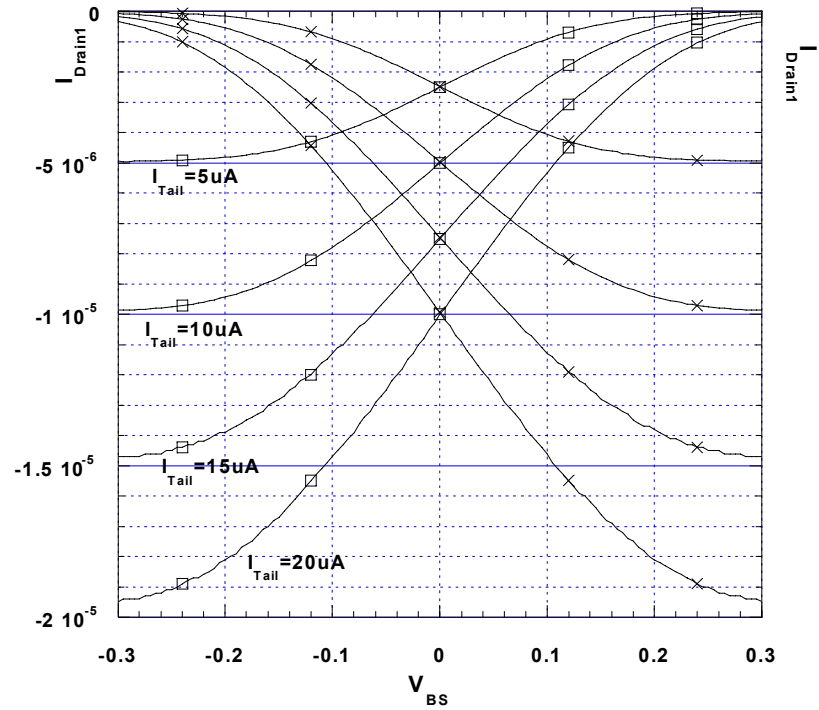
Appendix B: Additional BDDP Measured Data

B.1: Measured Data of BDDP with Aspect Ratio 10/4 m=12

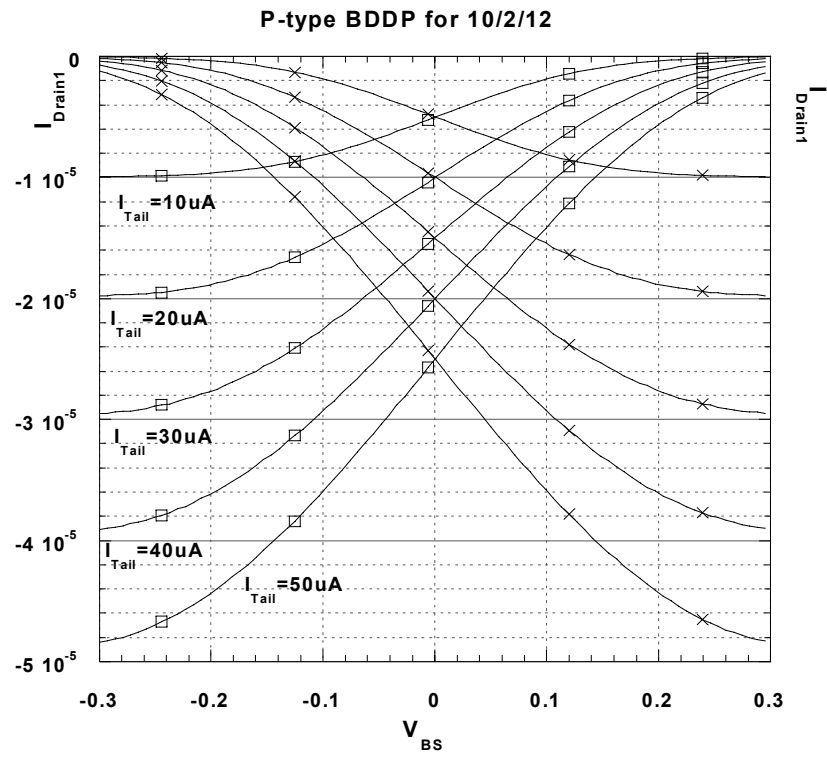
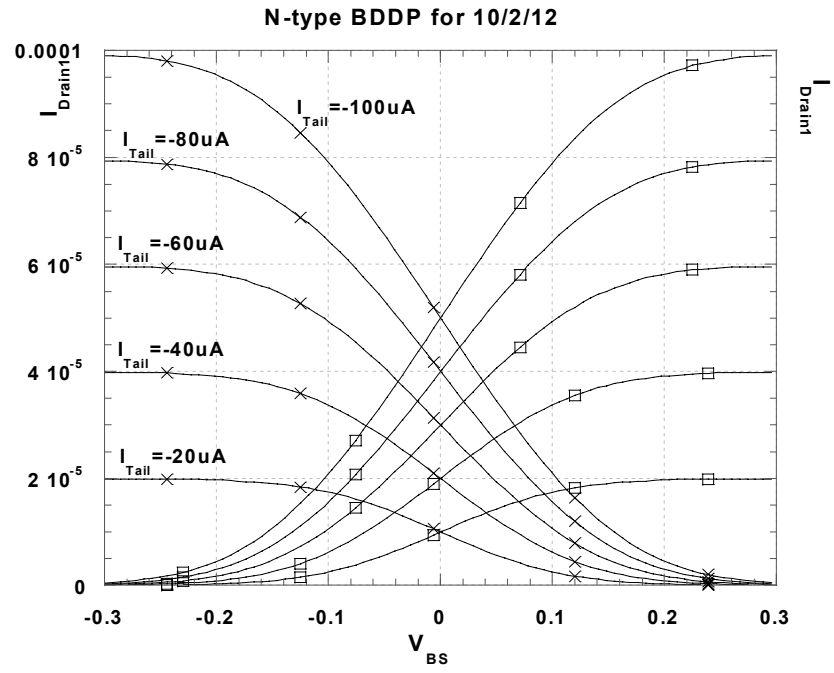
N-type BDDP for 10/4/12



P-type BDDP for 10/4/12

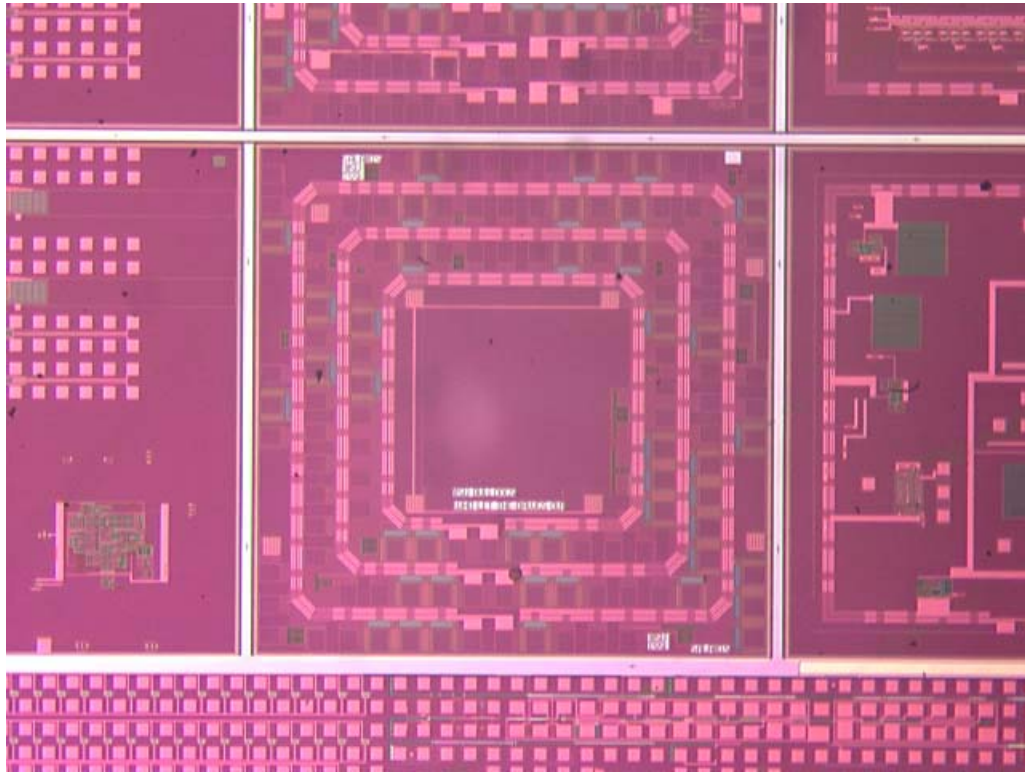


B.2: Measured Data of BDDP with Aspect Ratio 10/2 m=12

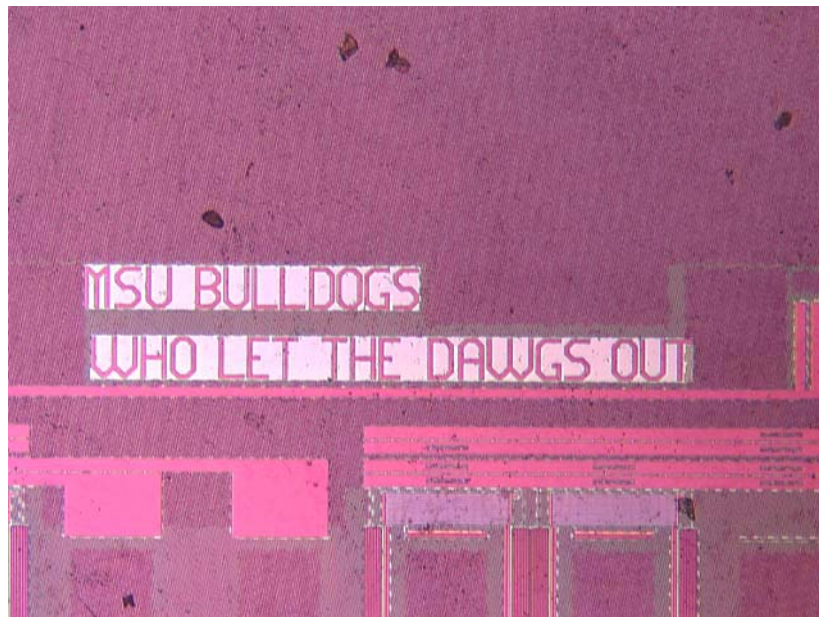


Appendix C: Test Setup and Microphotographs

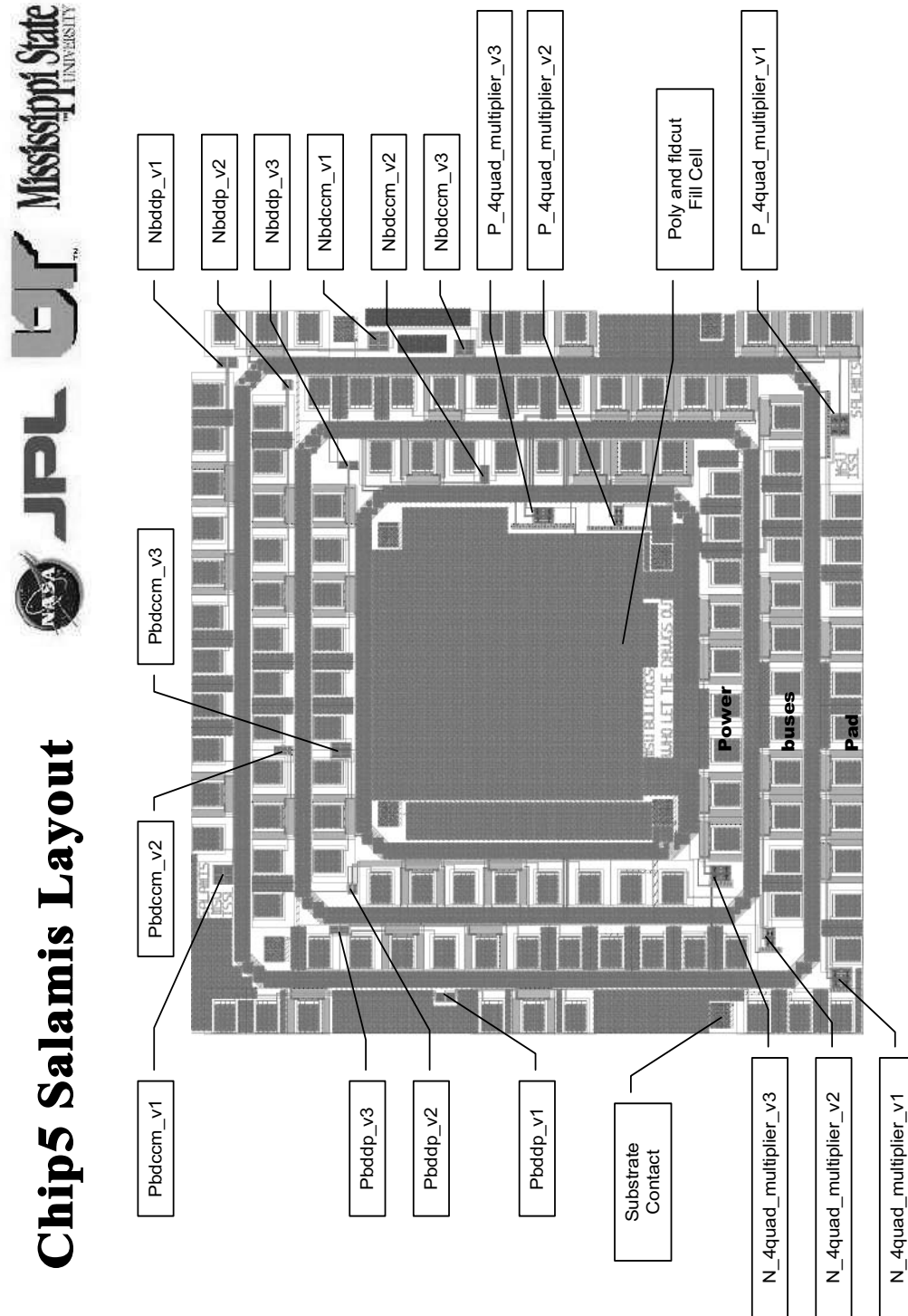
C.1: Full Chip Pictures



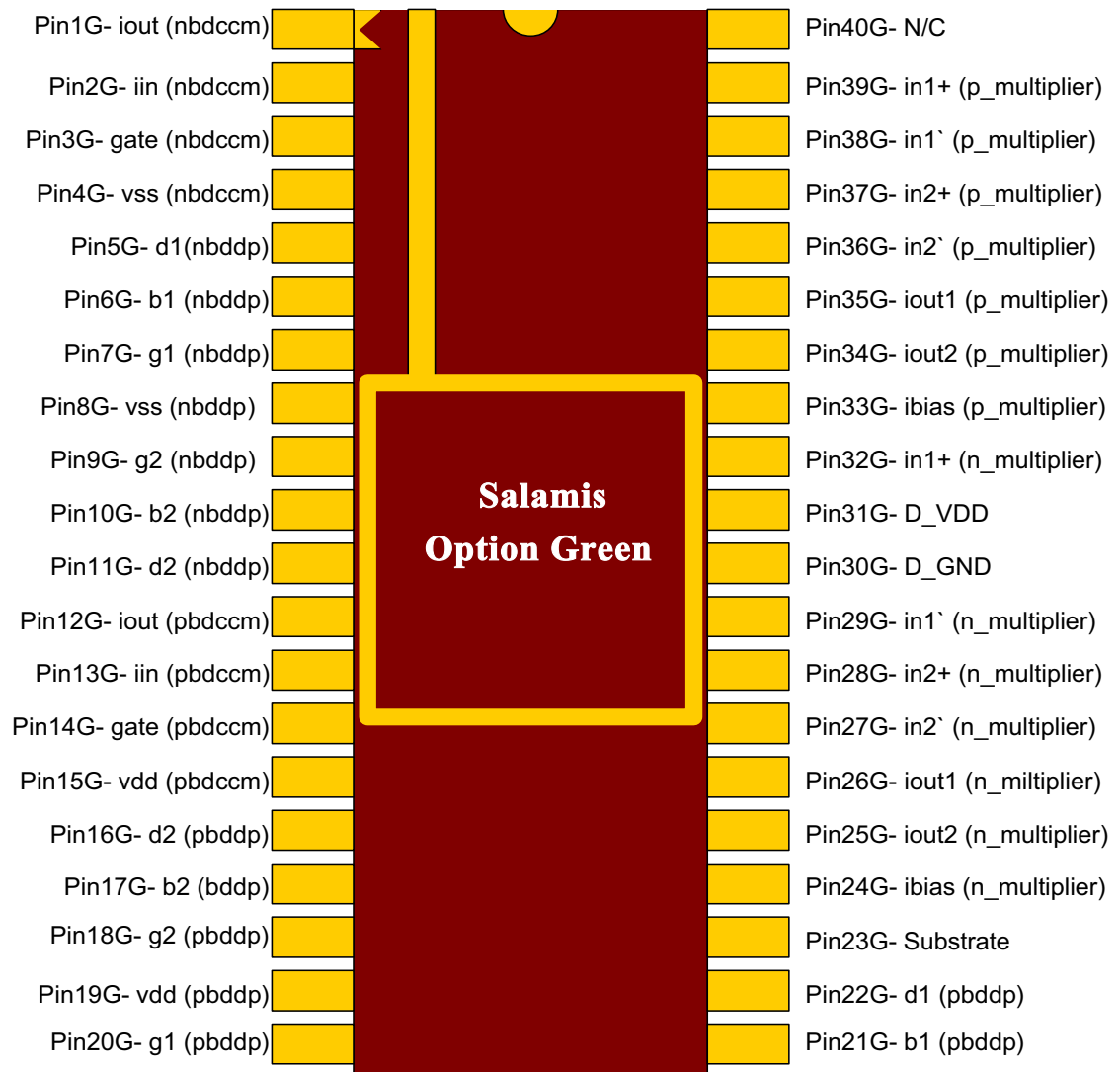
C.2: Zoomed-in Chip Picture



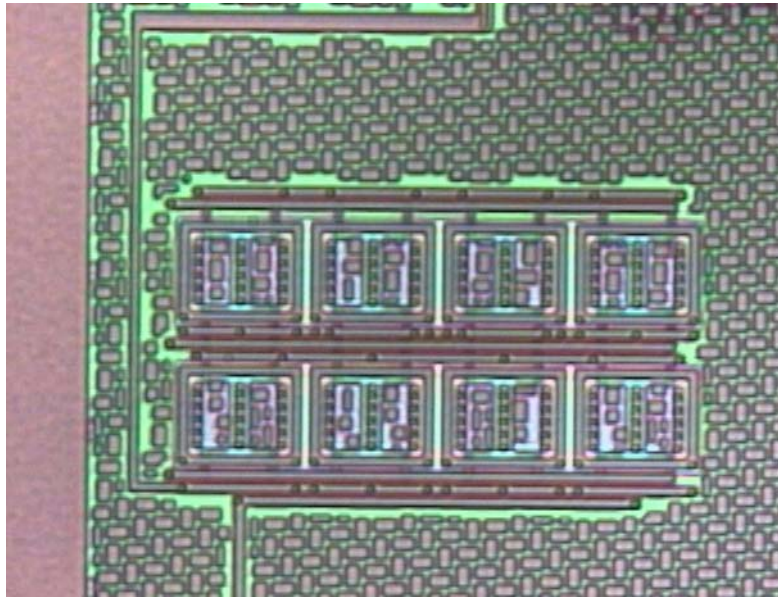
C.3: Full Chip Layout with Description



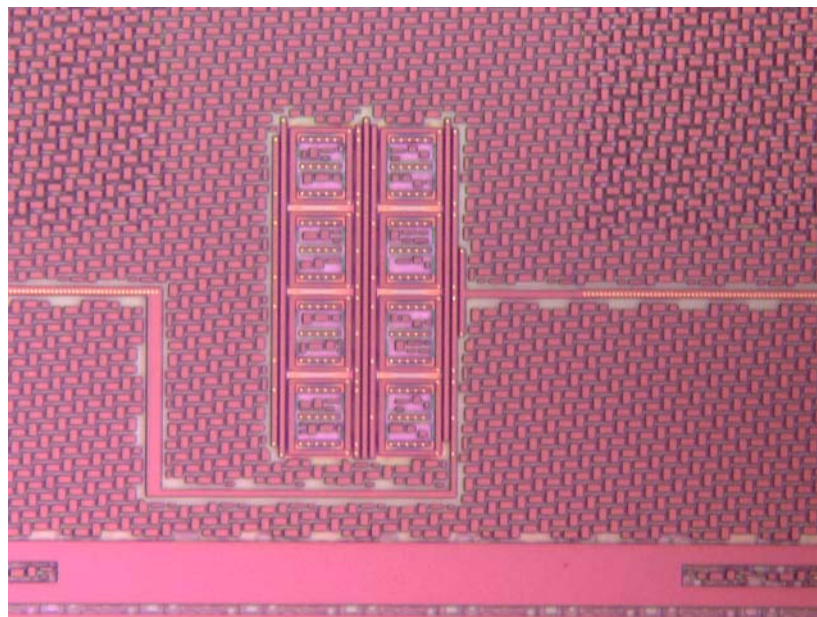
C.4: Block Diagram of 40-pin Dip Package



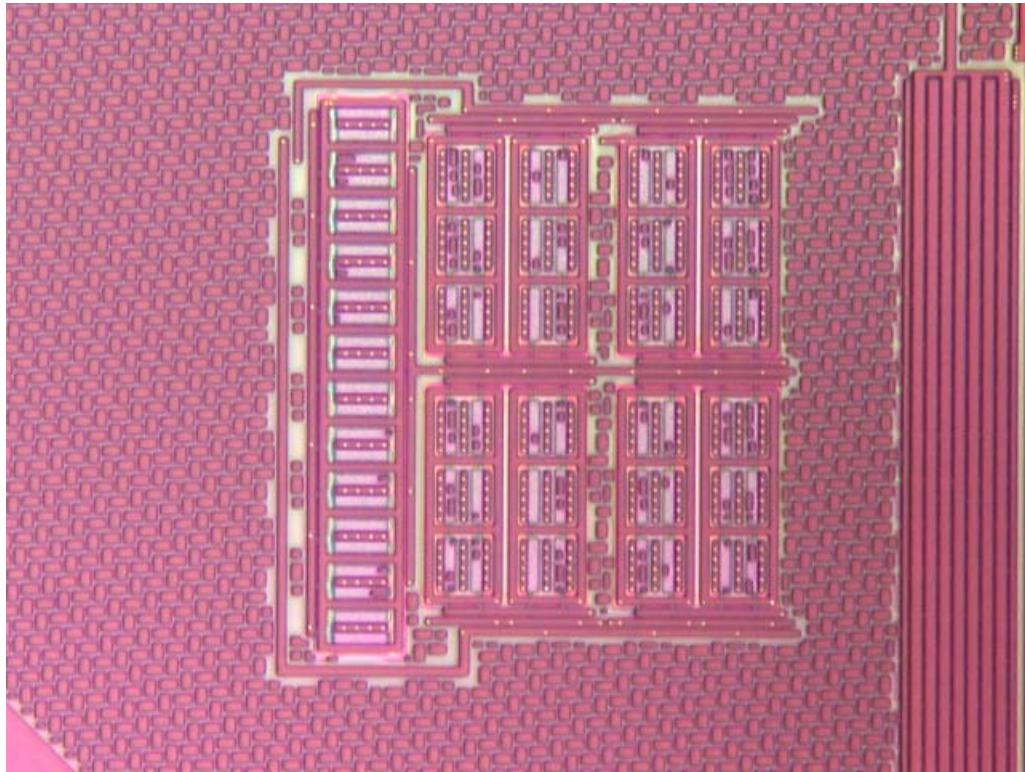
C.5: N-type BDCCM Picture



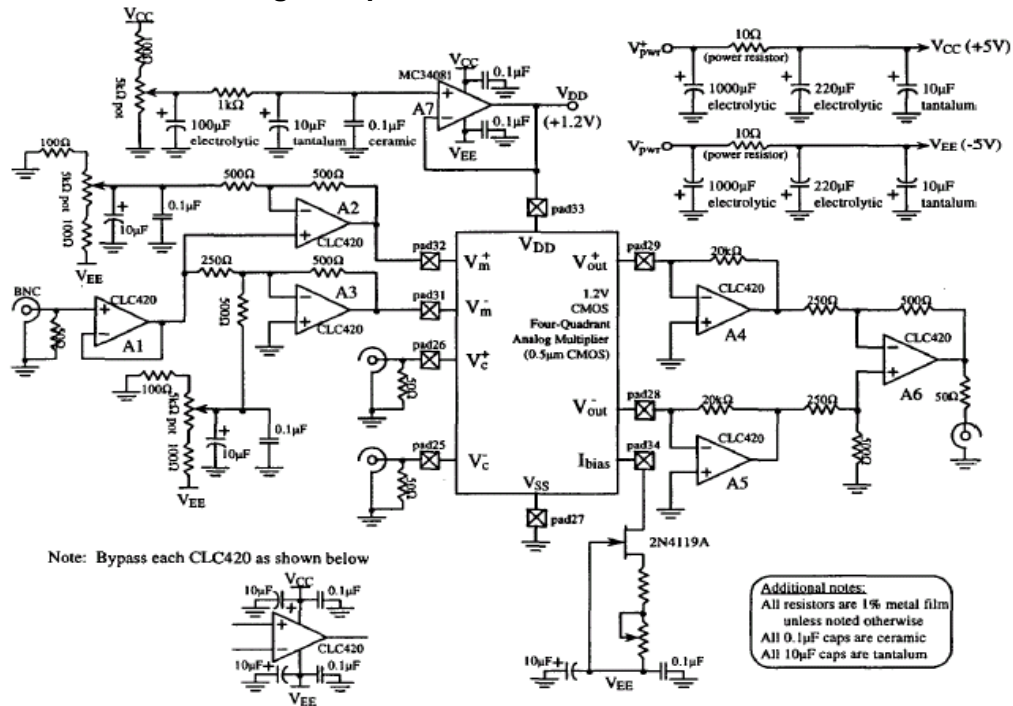
C.6: P-type BDCCM Picture



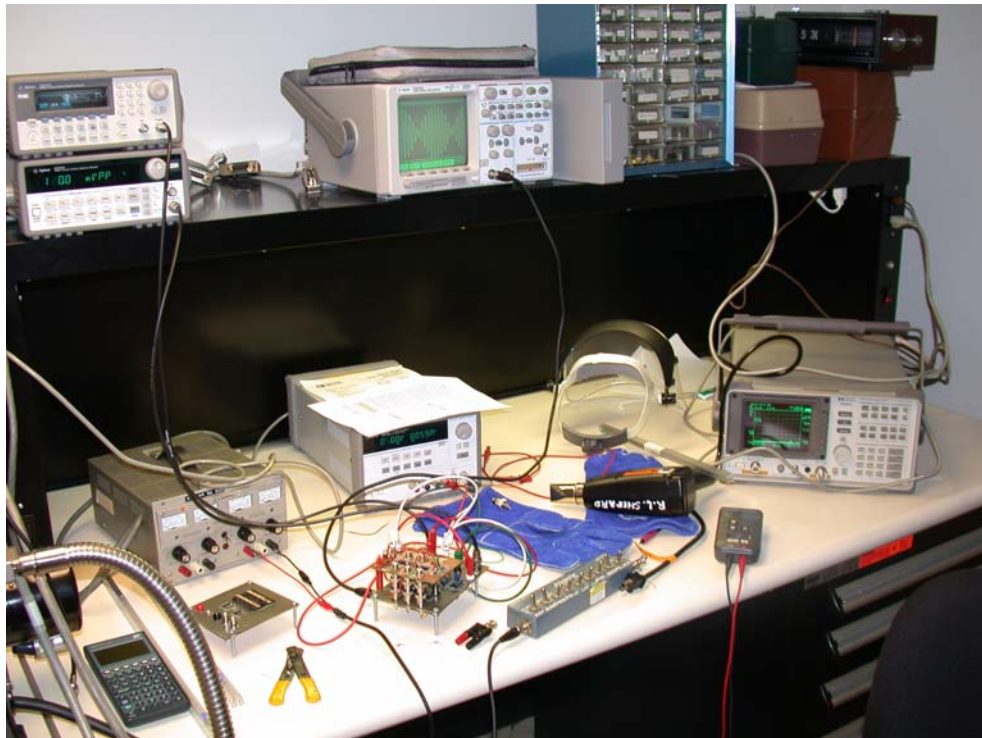
C.7: N-type 4-Quadrant Analog Multiplier



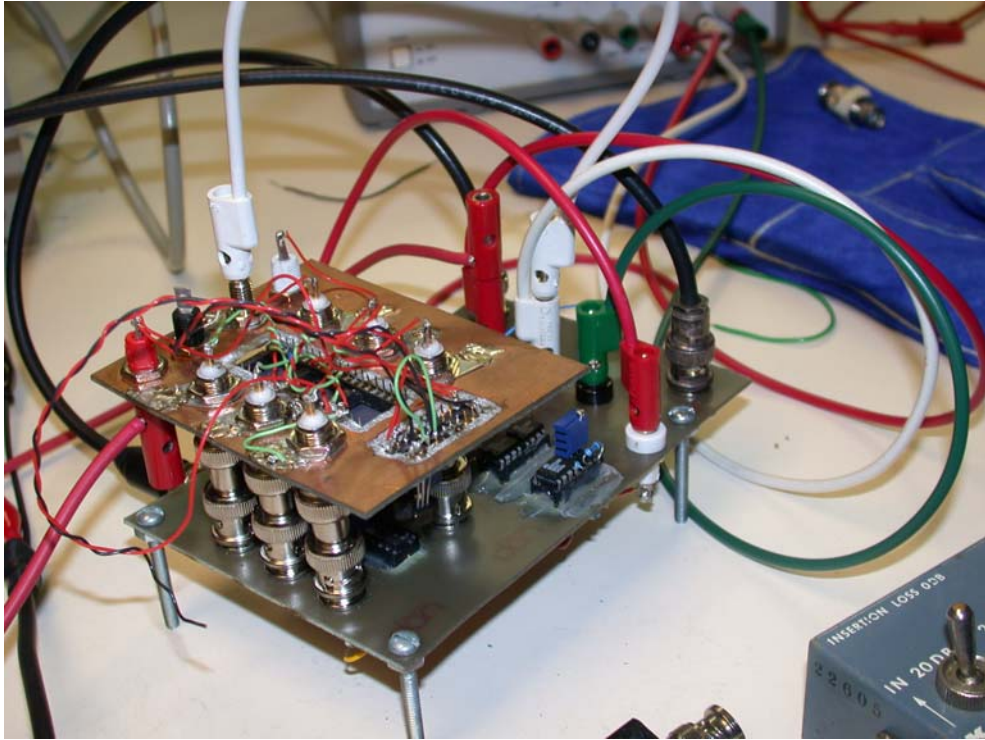
C.8: 4-Quadrant Analog Multiplier Test Board Schematic



C.9: 4-Quadrant Analog Multiplier Test Setup Picture



C.10: 4-Quadrant Analog Multiplier Test Setup Picture (zoom-in)



Vita

LeeKee (Ricky) Yong was born in Tawau, Malaysia in 1976. He attended elementary and high school at Chinese Academy of Malaysia. After graduating in 1997, he began studies at the Inti College, of Subang Jaya, Malaysia majoring in Electrical Engineering. He transferred to Mississippi State University, Mississippi in 1998 and received his Bachelor degree in Computer Engineering in fall of 2000. During his undergraduate education, he participated in summer internships, working 3 summers as a door to door sales person with Thomas Nelson Inc. Nashville, TN. He was also elected as the President of Malaysian Student Association of Mississippi State University during his senior year.

For his graduate education, Ricky accepted the research assistantship offered by Dr. Benjamin and sponsored by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with National Aeronautical and Space Administration (NASA). His main research focus has been Mixed signal CMOS design in partially-depleted SOI technology and developing technology files to support Cadence IC design tools. After completion of the M.S. degree in Electrical Engineering from UT (August 2002 target date), Ricky will work as a CAD design engineer at Analog Devices Inc. His hobbies and interests include computers, internet development, basketball, badminton, hiking, and jungle tracking.